

RISC-V Embedded Processor IP Cores

Efficient, Reliable, and Royalty-Free

Features	BA51 Ultra-Low-Power	BA53 Low-Power & Fast	EMSA5 Base	EMSA5-FS Functional Safety
ISA	RV32 [I/E]	RV32 [I/E]	RV32 [I/E]	RV32 [I/E]
ISA Extension Options				
Compressed Instr. (C)	Yes	Yes	Yes	Yes
Multiplication & Division (M)	Yes	Yes	Yes	Yes
Code Size Reduction (Zc)*	Yes	Yes	No	No
Single Precision Floating Point (F)	Yes	Yes	Yes	Yes
Double Precision Floating Point (D)	Yes	Yes	Yes	Yes
Atomic Instructions (A)	Yes	Yes	Yes	Yes
User-Level Interrupts (N)	Yes	Yes	No	No
Control & Status Reg. (Zcsr)	Yes	Yes	Yes	Yes
Instruction Fence (Zicsr)	Yes	Yes	Yes	Yes
Vector Instructions	On-Request	On-Request	Yes**	Yes**
Custom Instructions	Yes (option)	Yes (option)	No	No
Architecture	Harvard	Harvard	Harvard	Harvard
Pipeline Stages	2	5	5	5
Instruction TCM	Yes	Yes	Yes	Yes
Data TCM	Yes	Yes	Yes	Yes
Instruction Cache	Yes (option)	Yes (option)	Yes (option)	Yes (option)
Data Cache	No	No	Yes (option)	Yes (option)
Hardware Multiplier	Yes (option)	Yes (option)	Yes (option)	Yes (option)
Hardware Divider	Yes (option)	Yes (option)	Yes (option)	Yes (option)
Memory Protection Unit (MPU)	Yes (option)	Yes (option)	Yes (option)	Yes (option)
Floating Point Unit (FPU)	HP*, SP, DP	HP*, SP, DP	SP, DP	SP, DP
SoC Bus Protocol	AXI4	AXI4	AHB-Lite	AHB-Lite
Dual Core Lockstep	No	No	No	Yes (option)
Triple Modular Redundancy	No	No	No	Yes (option)
ISO 26262	-	-	-	ASIL-D
Coremarks / MHz	3.00	2.53	2.43	2.43
Fmax @ 22nm	400 MHz	1 GHz	800 MHz	500 MHz
Area @ in Eq. Gates	16k	30k	23k	77k
RV JTAG & Trace	Yes (option)	Yes (option)	Yes (option)	Yes (option)
Configurable Subsystem	Yes (option)	Yes (option)	Yes (option)	Yes (option)
Royalty-Free Licensing	Yes	Yes	Yes	Yes

* Non ratified RV ISA extension

** Partial support

