The ASCON-F IP core is a compact, high-throughput hardware engine implementing the lightweight authenticated encryption with associated data (AEAD) and hashing algorithms described in the Ascon v1.2 specification.

A single instance of the ASCON-F IP core can encrypt or decrypt data using the Ascon-128 and Ascon-128a functions or perform cryptographic hashing Hash per the Ascon-Hash and Ascon-Hasha functions. The mode of operation (encryption or decryption, and Ascon function), as well as the encryption key and nonce values, are runtime programmable and can be changed per block of input data. The core uses simple input and output interfaces, that can be optionally bridged to AXI4-Stream, or to AXI4 Memory Mapped master or slave ports using bridges separately available from CAST.

The core synthesizes to approximately 11k gates and is able to run at frequencies exceeding 2 GHz in modern ASIC technologies. Ignoring overheads related to input padding and core initialization, the throughput ranges from 5.3 to 16 bits/cycle depending on the mode and function, which at 2 GHz translates to 10.6 to 32 Gbps. The processing throughput can be further scaled by instantiating the core multiple times.

The core is designed for ease of use and integration and adheres to industry-best coding and verification practices. Technology mapping and timing closure are trouble-free, as the core contains no multi-cycle or false paths and uses only rising-edge-triggered D-type flip-flops, no tri-states, no SRAMs, and a single-clock/reset domain.

**About ASCON**

The ASCON family of algorithms was developed by Graz University of Technology, Infineon Technologies, Lamarr Security Research, and Radboud University and was selected in February 2023 by the US National Institute of Standards and Technology (NIST) as the new standard for lightweight cryptography. Learn more online at NIST, Wikipedia, and the Ascon website by Graz University of Technology.

**Block Diagram**

The core is available in RTL source or as a targeted FPGA netlist. It is delivered with everything required for a successful implementation, including a sophisticated, self-checking HDL Testbench, a behavioral C Model & test vector generator, and comprehensive documentation.

**Deliverables**

This core implements encryption functions and as such it is subject to export control regulations. Export to your country may or may not require a special export license. Please contact CAST to determine what applies in your specific case.
Applications

Implementing the Ascon family of lightweight authenticated ciphers and hash functions, the core can be used to protect edge IoT devices, secure communications or video surveillance systems, and encrypt data storage.

Implementation Results

The ASCON-F IP core can be mapped to any ASIC technology or FPGA device. The following are sample ASIC pre-layout results reported from synthesis with a silicon vendor design kit under typical conditions, with all core I/Os assumed to be routed on-chip.

<table>
<thead>
<tr>
<th>ASIC Technology</th>
<th>Logic (eq. gates)</th>
<th>Memory (bits)</th>
<th>Freq. (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC 7nm</td>
<td>10,544</td>
<td>0</td>
<td>2,300</td>
</tr>
<tr>
<td>TSMC 16nm</td>
<td>10,584</td>
<td>0</td>
<td>2,150</td>
</tr>
<tr>
<td>TSMC 28nm HPC</td>
<td>11,283</td>
<td>0</td>
<td>1,900</td>
</tr>
</tbody>
</table>

The provided figures do not represent the higher speed or smaller area for the core. Please contact CAST to get characterization data for your target configuration and technology.