The LIN-CTRL core is a communication controller that transmits and receives complete LIN frames to perform serial communication according to the LIN Protocol Specification. The LIN controller can be implemented as a master or as a slave and operate on LIN 1.3, 2.0, 2.1, or 2.2 LIN network. It uses a single master/multiple slave concept for message transfer between nodes of the LIN network. The message transfer can be controlled via a microcontroller interface and a LIN transceiver is needed for the connection to the LIN bus.

The LIN-CTRL core is a microcode-free design developed for reuse in ASIC and FPGA implementations. The scan-ready design is strictly synchronous with positive-edge clocking and no internal tri-states. The robustly verified core has been production-proven multiple times.

The LIN controller core is available in two versions: Standard, and Safety-Enhanced. The Safety-Enhanced version implements ECC for SRAMs protection and uses spatial redundancy for protecting the inner logic of the core. The Safety-Enhanced versions are certified as ISO-26262 ASIL-D Ready.

Applications
The LIN-CTRL core is used to interface sensors and actuators in a variety of applications such as automotive, industrial, and home appliances.

Block Diagram

Functional Description
The LIN-CTRL core is partitioned into modules as shown in the block diagram.

Host Controller Interface
This interface is responsible for handling the communication with the host controller of the system.

Register Block
The Register Block provides control registers and status registers to control the LIN message transfer. Access to the registers is possible via the host controller interface.

Data Buffer
The 8-byte Data Buffer stores the data that has to be sent with the current LIN frame or the data that has been received with the last LIN frame. Access to the Data Buffer is possible via the host controller interface.

FEATURES
- Support of LIN specifications 2.0, 2.1, and 2.2A
  - Backward compatible with LIN specification 1.3
- Configurable for support of master or slave functionality
- Programmable data rate between 1 Kbit/s and 20 Kbit/s (for master)
- Automatic bit-rate detection (for slave)
- 8-byte data buffer
- Generic 8-bit microcontroller interface
  - Wrappers converting the generic microcontroller interface to AMBA APB or AHB are offered with the core
- Slave can be implemented with or without clock synchronization
- Fully synchronous design, available in VHDL or Verilog, completely synthesizable
- The LIN Controller synthesizes to approximate 250 to 400 ALMs depending on the configuration
- Robustly verified and multiple times production-proven IP core
- Safety-Enhanced Version (optional)
  - Certified as ISO-26262 ASIL-D Ready
  - Implements ECC for SRAM and spatial redundancy for inner logic protection
Functional Description (cont.)

Control FSM
The finite control state machine is responsible for the behavior of the core depending on host controller commands and bus activity. It generates and processes the LIN frame fields according to the LIN protocol.

Bit Stream Processor
This module converts the data stream from parallel to serial (from transmit buffer to bus) and from serial to parallel (from bus to receive buffer).

Bit Timing Logic
The Bit Timing Logic is responsible for synchronizing the received data stream from the bus with the internal bit time clock.

Implementation Results
The LIN-CTRL core can be mapped to any Intel® FPGA device (provided sufficient silicon resources are available) and optimized to suit the particular project’s requirements. The following are sample implementation data for the core assuming all I/Os are routed off-chip.

<table>
<thead>
<tr>
<th>Family / Device</th>
<th>Mode</th>
<th>Logic Resources</th>
<th>Fmax² (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arria 10</td>
<td>Master</td>
<td>228 ALMs</td>
<td>446</td>
</tr>
<tr>
<td>10AS016C3U19I2LG</td>
<td>Slave¹</td>
<td>361 ALMs</td>
<td>297</td>
</tr>
<tr>
<td>Cyclone 10 LP</td>
<td>Master</td>
<td>492 LEs</td>
<td>187</td>
</tr>
<tr>
<td>10CL010YU256C6G</td>
<td>Slave¹</td>
<td>833 LEs</td>
<td>161</td>
</tr>
<tr>
<td>Max 10</td>
<td>Master</td>
<td>497 LEs</td>
<td>148</td>
</tr>
<tr>
<td>10M08DAF484I7G</td>
<td>Slave¹</td>
<td>811 LEs</td>
<td>141</td>
</tr>
</tbody>
</table>

Notes:
1) Slave implemented with clock synchronization
2) Minimum clock frequency for the LIN controller is 8 MHz

Core Modifications
The LIN core can be modified to include an acceptance filter. With that, a simple LIN slave that transmits response frames for only one identifier could be realized without the assistance of a host controller.

Support
The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification
The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

Deliverables
The core is available in synthesizable RTL and FPGA netlist forms. It ships with everything required for successful implementation, including:

- VHDL or Verilog RTL source code, or targeted FPGA netlist
- Testbenches for behavioral, and post-synthesis verification
- Simulation and Synthesis scripts
- Low-Level Hardware Abstraction Layer (HAL)
- Optional MISRA C non-OS, bare-metal driver with advanced software examples
- User Documentation and RUVM register descriptions.

The optional safety-enhanced package further includes the Safety Manual (SAM), a Failure Modes, Effects and Diagnostics Analysis (FMEDA) and the ASIL-D Ready certificate, issued by SGS-TÜV Saar GmbH.