ZipAccel-C

GZIP/ZLIB/Deflate Data Compression Core

ZipAccel-C is a custom hardware implementation of a lossless data compression engine that complies with the Deflate, GZIP, and ZLIB compression standards.

The core receives uncompressed input files and produces compressed files. No post processing of the compressed files is required, as the core encapsulates the compressed data payload with the proper headers and footers. Input files can be segmented, and segments from different files can be interleaved at the core's input.

The core's flexible architecture enables fine-tuning of its compression efficiency, throughput, and latency to match the requirements of the end application. Throughputs in excess of 200 Gbps are feasible in FPGAs, and latency can be as small as a few tens of clock cycles.

ZipAccel-C offers compression efficiency practically equivalent to today's popular deflate-based software applications. Analyzing processing speed versus compression efficiency to achieve the best tradeoff for a specific system is facilitated by the included software model, and by support from our team of data compression experts.

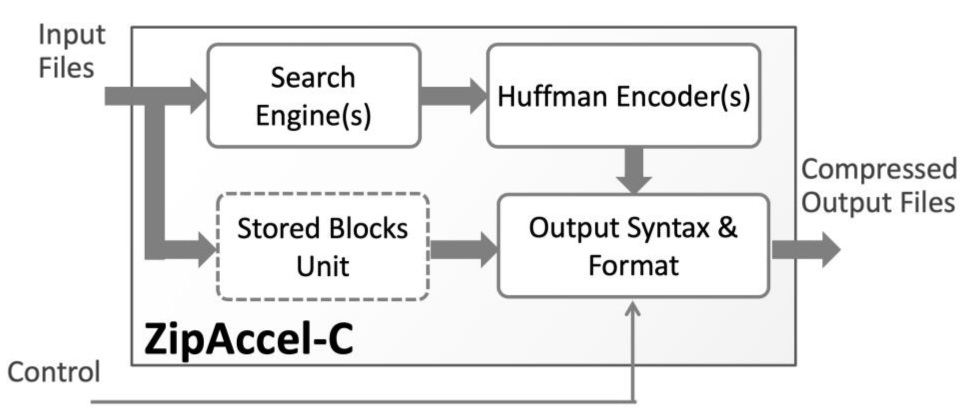
ZipAccel-C has been designed for ease of use and integration. It operates on a standalone basis, off-loading the host CPU from the demanding task of data compression, and optionally from the task of encrypting the compressed stream. Streaming AXI-Stream or native FIFO-like data interfaces ease SoC integration.

Technology mapping is straightforward, as the design is scan-ready, LINT-clean, microcode-free, and uses easily replaceable, generic memory models. Memory blocks can optionally support Error Correction Codes (ECC) to simplify achievement of Enterprise-Class reliability requirements. Furthermore, input file segmentation can limit the inter-file latency and helps users achieve Quality of Service (QoS) objectives.

Applications

The ZipAccel-C core is ideal for increasing the bandwidth of optical, wired or wireless data communication links, and for increasing the capacity of data storage in a wide range of devices such as networking interface/routing/storage equipment, data servers, or SSD drives. The core can also help reduce the power consumption and bandwidth of centralized memories (e.g. DDR) or interfaces (e.g. Ethernet, Wi-Fi) in a wide range of SoC designs.

Block Diagram



FEATURES

Compression Standards

- Deflate (RFC-1951)
- ZLIB (RFC-1950)
- GZIP (RFC-1952)

Deflate Features

- LZ77 with configurable block and search window size
- Static and dynamic Huffman
- Optional stored deflate blocks
- Dynamic mode selection

Flexible Architecture

- Fine-tune throughput, compression efficiency, and latency to match application requirements
  - More than 200Gbps with one core instance, scalable to meet any throughput requirement
  - Compression efficiency can be on par with Unix/Linux max compression option (gzip -9)
  - Silicon requirements start from less than 100k gates
  - Under 40 clock cycles for static Huffman
- Configuration options (partial list):
  - Search engine and Huffman encoder architecture
  - History search window size (up to 32kb)
  - Deflate block size
  - Stored blocks support
  - Parallel processing level

Easy to Use and Integrate

- Processor-free, standalone operation
- Streaming AXI-Stream or native FIFO-like data interfaces
- Large file segmentation enables meeting QoS objectives
- Microcode-free, LINT-clean, scan-ready design
- Optional ECC memories
- Optionally integrated with DMA, encryption or other cores from CAST
- Complete, turn-key Accelerator Designs available on Intel® FPGA boards

Implementation Results

ZipAccel-C reference designs have been evaluated in a variety of technologies. ZipAccel-C performance can scale by instantiating more search engines and/or Huffman encoders. Furthermore, other design options such as the search area window affect the silicon resources utilization.

The following are sample Intel® FPGA results for a subset of the possible configuration options, and do not represent the smallest possible area requirements nor the highest possible clock frequency.

Family	Configuration	ALMs	RAM Bits
Agilex (-3)	1 Systolic Search Engine, 1 Static Huffman Encoder, 512B Window, 450MHz	7,021	2,040
Arria 10 GX (-3)	1 Systolic Search Engine, 1 Static Huffman Encoder, 2kB History, 320MHz	13,641	5,656
Arria 10 GX (-3)	1 Hash Search Engine, 1 Dynamic Huffman Encoder, 8kB History, 210MHz	40,668	683,581
Agilex (-3)	1 Hash Engine, 1 Dynamic Huffman Encoder, 32KB History, 250MHz	17,091	1,390,662
Arria 10 GX (-3)	4 Hash Search Engines, 1 Dynamic Huffman Encoder, 4KB History, 110MHz	64,044	1,513,623
Agilex (-3)	26 Systolic Search Engines, 26 Static Huffman Encoders, 2kB History, 450MHz	438,617	2,055,946
Agilex (-1)	30 Search Engines, 10 Static Huffman Encoders, 256B History, 500MHz	319,724	7,471,974

Please contact CAST Sales to get characterization data for your target application and technology.

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has also been embedded in several commercially-shipping products and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in synthesizable HDL (System Verilog) or targeted FPGA netlist forms and includes everything required for successful implementation. Its deliverables include:

- Sophisticated Test Environment.
- Simulation scripts, test vectors and expected results
- Synthesis script
- Comprehensive user documentation

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.