

UDPIP-40G/50G

40G/50G UDP/IP Hardware Protocol Stack

Implements a UDP/IP hardware protocol stack that enables high-speed communication over a LAN or a point-to-point connection. Designed for standalone operation, the core is ideal for offloading the host processor from the demanding task of UDP/IP encapsulation and enables media streaming with speeds up to 50Gbps even in processor-less SoC designs.

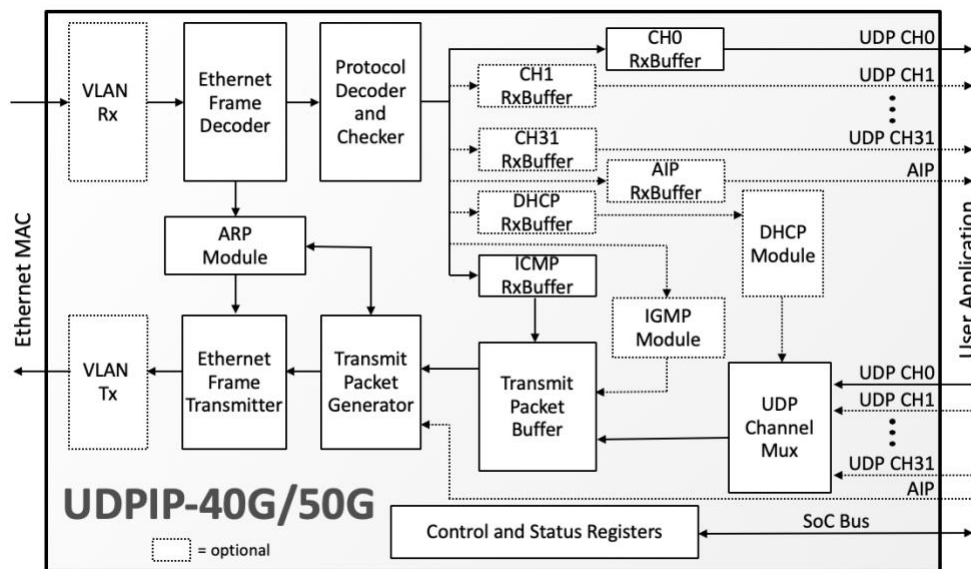
Trouble-free network operation is ensured through run-time programmability of all the required network parameters (local, destination and gateway IP addresses; UDP ports; and MAC address). The core implements the Address Resolution Protocol (ARP), which is critical for multiple access networks, and the Echo Request and Reply Messages (“ping”) of the Internet Control Message Protocol (ICMP) widely used to test network connectivity. It can use a static IP address or automatically request and acquire an IP address from a Dynamic Host Configuration Server (DHCP) server. Furthermore, the core supports 801.1Q tagging and is suitable for operation in a Virtual LAN.

The core is easy to integrate into systems with or without a host processor. Packet data can be read/written to the core via dedicated streaming-capable interfaces, or optionally via registers mapped on an SoC bus. The AMBA® AXI4-stream or the Avalon®-ST streaming protocols and the AMBA AHB and AXI, Avalon-MM, or Wishbone SoC bus protocols are supported.

Applications

Video, image and audio streaming or broadcasting over Ethernet, in devices such as IP cameras compatible to the GigE Vision, ONVIF, or PSIA standards, VOIP and smart phones. Also, high-frequency trading systems, high-speed communication between LAN nodes, device monitoring, and control over IP networks.

Block Diagram



FEATURES

Complete UDP/IP Hardware Stack

- 10G, 40G, and 50G Ethernet
- IPv4 support without packet fragmentation
- Jumbo and Super Jumbo Frames
- Transmit and Receive
- ARP with Cache
- ICMP (Ping Reply)
- IGMPv3 (Multicast)
- UDP/IP Unicast and Multicast
- UDP Port Filtering
- UDP/IP Checksums generation and validation, and optional Ethernet CRC validation
- VLAN (IEEE 802.1Q) support
- 1 to 32 UDP transmit and 1 to 32 UDP receive channels
- Ethernet Framing processing for non-UDP user-provided packets
- DHCP client

Trouble-Free Operation

- Run time programmable network parameters
 - Local MAC address, Local IP address, Gateway IP address, and IP subnet mask
 - Per-channel: Destination IP address, Source and Destination and filtered UDP ports, multicast enable/disable and receive group
- ARP support for operation in networks with Dynamic IP allocation

Easy SoC Integration

- Flexible interfaces:
 - Packet Data: 256-bit streaming capable using Avalon-ST or AXI4-Stream
 - Control/Status Registers: Generic 32-bit SRAM-like, or optionally 32-bit AHB, AXI, Avalon-MM or Wishbone
- Separate clock domains for packet processing and control/status interfaces
- Configurable buffer sizes
- Rich interrupt support for system events

Functional Description

The UDPIP-40G/50G core receives and transmits UDP packet data, and forwards other traffic from the Ethernet MAC to the application and vice versa. It also receives and transmits ARP requests and responses, and responds to ICMP echo reply messages. The core generates and validates the UDP and IP checksums of outgoing and incoming packets, respectively. It can be programmed to discard or forward corrupted packets to the user application.

The core consists of the following modules:

The **Ethernet Frame Decoder** receives Ethernet frames from an external Ethernet MAC, detects the frame type and sends frames to the ARP or the IP packet decoder.

The **Ethernet Frame Transmitter** provides the external Ethernet MAC interface. The transmitter also multiplexes ARP and IP transmit packets from the core subsystems.

The **VLAN Receiver** receives Ethernet frames from an external Ethernet MAC, and when enabled detects and compares VLAN tag & filters frames to the correct VLAN tag.

The **VLAN Transmitter** receives Ethernet frames from the Ethernet Frame Transmitter and adds the VLAN Tag to the frames when enabled.

The **Protocol Decoder and Checker** receives IP packets and handles them according to the packet type. The module decodes ICMP/IGMP/UDP/IP Packet types and saves the packets to the related receive packet buffer. The module also checks packets for errors.

The **Received Packet Buffers** implement separate data storage for each protocol and UDP channels. The buffers are implemented if the related protocol or UDP channel is enabled. The buffer sizes are configurable at synthesis time.

The **Transmit Packet Buffer** stores UDP application data as well as the ICMP and IGMP packet data. The size of the buffer is configurable at synthesis time.

The **Transmit Packet Generator** assembles ICMP, IGMP, UDP packets based on data received from the Transmit Packet Buffer.

The **ARP Module** sends and receives ARP packets and handles the packets according to command in the packet.

The **DHCP Module** automatically requests and acquires an IP address from a DHCP server.

Finally, the **Control and Status Registers** control the core functionality and reports the core status.

Implementation Results

UDPIP-40G/50G reference designs have been evaluated in a variety of technologies. The following are sample ASIC pre-layout results reported from synthesis with a silicon vendor design kit under typical conditions, with all core I/Os assumed to be routed on-chip. The sample results do not represent the highest speed or smallest area for the core.

UDP Channels	ASIC Technology	Eq. NAND2 gates	Fmax (MHz)	Memory (Bytes)
1	TSMC 65nm	42011	333	48kB
1	TSMC 90nm	40269	333	96kB
4	TSMC 65nm	47552	333	48kB
4	TSMC 90nm	45170	333	96kB

Table 1: UDPIP-40G/50G sample results for the core configured with a 256-bit AXI4-Stream data-path, ARP, ICMP, IGMP, Rx and Tx.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts and comprehensive user documentation.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.