**UDPIP-1G**

1G UDP/IP Hardware Protocol Stack Core

Implements a UDP/IP hardware protocol stack that enables high-speed communication over a LAN or a point-to-point connection. Designed for standalone operation, the core is ideal for offloading the host processor from the demanding task of UDP/IP encapsulation and enables media streaming with speeds up to 1 or 10Gbps, depending on the speed of the silicon fabric, even in processor-less SoC designs.

 Trouble-free network operation is ensured through run-time programmability of all the required network parameters (local, destination and gateway IP addresses; UDP ports; and MAC address, etc). The core implements the Address Resolution Protocol (ARP), which is critical for multiple access networks, and the Echo Request and Reply Messages (“ping”) of the Internet Control Message Protocol (ICMP) widely used to test network connectivity. It can use a static IP address or automatically request and acquire an IP address from a Dynamic Host Configuration Server (DHCP) server. Furthermore, the core supports 801.1Q tagging and is suitable for operation in a Virtual LAN.

The core is easy to integrate into systems with or without a host processor. Packet data can be read/written to the core via dedicated AMBA® AXI4-stream or Avalon®-ST interfaces, while registers are accessible via an AXI4-Lite, or AHB or Avalon-MM slave interface. Bridges to other interface protocols can be made available upon request. The core is Ethernet MAC-independent but can be made available pre-integrated with an Altera, Xilinx, or other third-party eMAC core.

**Applications**

Video, image and audio streaming or broadcasting over Ethernet, in devices such as IP cameras compatible to the GigE Vision, ONVIF, or PSIA standards, VOIP and smart phones. Also high-frequency trading systems, high-speed communication between LAN nodes, device monitoring, and control over IP networks.

**Block Diagram**
Functional Description

The UDPIP-1G core receives and transmits UDP packet data, and forwards other traffic from the Ethernet MAC to the application and vice versa. It also receives and transmits ARP requests and responses, and responds to ICMP echo reply messages. The core generates and validates the UDP and IP checksums of outgoing and incoming packets, respectively. It can be programmed to discard or forward corrupted packets to the user application.

The core consists of the following modules:

The Ethernet Frame Decoder receives Ethernet frames from an external Ethernet MAC, detects the frame type and sends frames to the ARP or the IP packet decoder. The Ethernet Frame Transmitter provides the external Ethernet MAC interface. The transmitter also multiplexes ARP and IP transmit packets from the core subsystems.

The VLAN Receiver receives Ethernet frames from an external Ethernet MAC, and when enabled detects and compares VLAN tag & filters frames to the correct VLAN tag.

The VLAN Transmitter receives Ethernet frames from the Ethernet Frame Transmitter and adds the VLAN Tag to the frames when enabled.

The Packet Receiver Module receives IP packets and handles them according to the packet type. The Packet Decoder receives IP packets and the decoded packets are stored in the Rx Packet Buffer and then passed to the user application. The Received Packet Buffer implements separate data storage for the UDP application data and other data, and its size is configurable at synthesis time.

The Packet Transmit Module assembles UDP and ICMP packets. The UDP application data, as well as the ICMP packet data, are stored in the transmit buffer, the size of which is configurable at synthesis time.

The ARP Module sends and receives ARP packets and handles the packets according to command in the packet. The DHCP Module automatically requests and acquires an IP address from a DHCP server.

The UDP Channel Demultiplexer receives UDP packets and demultiplexes them according to a decoded UDP channel number. The UDP Channel Multiplexer receives UDP packet channels from a user application and multiplexes them to the Packet Transmitter module.

Finally, the Control and Status Registers control the core functionality and report the core status.

Implementation Results

UDPIP-1G reference designs have been evaluated in a variety of technologies. The following are sample ASIC pre-layout results reported from synthesis with a silicon vendor design kit under typical conditions, with all core I/Os assumed to be routed on-chip. The sample results do not represent the highest speed or smallest area for the core.

<table>
<thead>
<tr>
<th>UDP Channels</th>
<th>ASIC Technology</th>
<th>Eq. NAND2 gates</th>
<th>Fmax (MHz)</th>
<th>Memory (Bytes)</th>
<th>Ethernet Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TSMC 65nm</td>
<td>28,926</td>
<td>333</td>
<td>16,640</td>
<td>10/100/1000 and 10G</td>
</tr>
<tr>
<td>1</td>
<td>TSMC 90nm</td>
<td>26,782</td>
<td>333</td>
<td>16,640</td>
<td>10/100/1000 and 10G</td>
</tr>
<tr>
<td>4</td>
<td>TSMC 65nm</td>
<td>36,308</td>
<td>333</td>
<td>24,832</td>
<td>10/100/1000 and 10G</td>
</tr>
<tr>
<td>4</td>
<td>TSMC 90nm</td>
<td>33,594</td>
<td>333</td>
<td>24,832</td>
<td>10/100/1000 and 10G</td>
</tr>
</tbody>
</table>

Table 1: UDPIP-1G sample results for the core configured with ARP, ICMP, IGMP, Rx and Tx, and without DHCP and VLAN support.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts, and comprehensive user documentation.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.