The TSN-SE implements a configurable controller meant to ease the implementation of switched endpoints for Time Sensitive Networking (TSN) Ethernet networks. It integrates hardware stacks for timing synchronization (IEEE 802.1AS-2020), traffic shaping (IEEE 802.1Qav and IEEE 802.1Qbv), frame-preemption (IEEE 802.1Qbu and IEEE 802.3br) and a low-latency Ethernet MAC. Enhanced reliability features can also be supported, using the optional hardware modules for Frame Replication and Elimination for Reliability (IEEE 802.1CB) and Per-Stream Filtering and Policing (IEEE 802.1Qci).

The controller core is designed to enable high-precision timing synchronization and flexible yet accurate traffic scheduling. With cut-through switching and minimal buffering even at the Ethernet MAC level, the TSN-SE features extremely low and deterministic ingress and egress latencies and simplifies the development of time-aware applications. Furthermore, it allows the system to define and tune in real time the traffic shaping parameters according to an application’s requirements, and provides the system with timing information (timestamps, alarms, etc.) that is typically required for the operation of a TSN network bridge or endpoint.

The TSN-SE uses standard AMBA® interfaces to ease integration. Its configuration and status registers are accessible via a 32-bit-wide APB bus, and packet data are input and output via AXI-Streaming interfaces with 32-bit data buses. To further expedite and ease the implementation of customer applications, CAST offers software stacks supporting higher-layer protocols, such as IEEE 802.1Qcc, IEEE 802.1Qca, and SNMP, as well as hardware integration and software porting services.

The TSN-SE is designed with industry best practices and is available in synthesizable RTL (Verilog 2001) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

**Applications**

The TSN-SE is suitable for the implementation of TSN Ethernet Endpoints in daisy-chained networks (e.g. ring topologies) requiring robust, low-latency, and deterministic communication. Such networks are used in automotive, industrial control, medical, and aerospace applications.
Implementation Results

The TSN-SE can be mapped to any AMD FPGA device (provided sufficient silicon resources are available). The FPGA resources requirements depend on the core configuration. The following are sample results for a small number of core configurations. Please contact CAST to get characterization data for your target configuration and technology.

<table>
<thead>
<tr>
<th>Family/Device</th>
<th>Config.*</th>
<th>Logic</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kintex 7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XC7k325-2</td>
<td>64 Lookup Entries 16kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth No Frame Preemption</td>
<td>12,253 LUTs</td>
<td>30 RAMB36 22 RAMB18</td>
</tr>
<tr>
<td></td>
<td>256 Lookup Entries 16kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth No Frame Preemption</td>
<td>14,922 LUTs</td>
<td>57 RAMB36 23 RAMB18</td>
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<tr>
<td>Kintex UltraScale</td>
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<td>17,941 LUTs</td>
<td>64 RAMB36 31 RAMB18</td>
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<td>XCKU3P-1-I</td>
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<td>18,262 LUTs</td>
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<td>4k Lookup Entries 8kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth Frame Preemption</td>
<td>78,176 LUTs</td>
<td>538 RAMB36 20 RAMB18</td>
</tr>
</tbody>
</table>

*TPartial list of configuration parameters

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The TSN-SE has been rigorously verified, hardware-validated, and tested in real-life environments. It has also been tested and verified at TSN interoperability plugfests organized by the Labs Network Industry 4.0 (LNI 4.0) association and the Industrial Internet Consortium (IIC).

Deliverables

The core includes everything required for successful implementation:

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation
- Lightweight PTP stack
- Device driver for FreeRTOS and Linux

Customers may optionally choose to license the TSN-SE core pre-integrated with a small, deeply embedded processor running the PTP stack.

Related Products

The core is a member of CAST’s family of automotive interface products that includes:

- TSN-EP TSN Ethernet Endpoint IP Core
- TSN-SW: TSN Ethernet Switch IP Core
- TSN-VIP TSN Ethernet Verification IP
- LLEMAC-1G Low-Latency 10/100/1000 Ethernet MAC IP core
- CAN 2.0/CAN FD/CAN XL Controller IP core
- CAN 2.0/CAN-FD Verification IP
- LIN 2.2/2.1/2.0 Master/Slave Controller IP core
- SENT / SAE J2716 Transmitter/Receiver Controller IP core