The I3C-S core implements a versatile MIPI® Improved Inter-
Integrated Circuit (I3C) Slave controller core suitable for any I3C bus
 topology & compliant with the latest MIPI I3C BasicSM specification.

The highly featured slave-only core
 communicates in Single Data Rate (SDR)
 mode, but can tolerate High Data Rate
 (HDR) traffic. It can coexist and
 communicate with legacy I2C devices,
 and it can optionally be configured to
 operate as such in an I3C or I2C bus. The
 I3C-S needs no firmware support to parse
 and execute the broadcast or direct
 Common Command Codes (CCCs)
 relevant to I3C Basic Slaves. It can be
 assigned a Dynamic Address by the bus
 master or use its legacy I2C static
 address, it supports Hot Join and is
 capable of generating In-Band Interrupts
 when directed by the host to do so.

Designed for easy integration, the I3C-S can operate in two different modes. Under normal
 mode, data from private I3C or legacy I2C write transfers are stored to a FIFO and made
 available to the host via an APB Slave interface. In a similar way, the host provides data to
 be used for private I3C or legacy I2C read transfers through the core’s AHB slave interface.
 Alternatively, the core can operate in I3C-to-AHB bridging mode, where it autonomously
 converts private I3C or legacy I2C transfers to accesses on its AHB master port using a
 simple yet configurable over-I3C protocol. Under the I3C-to-AHB bridging mode, the core
 needs no software assistance and provides the I3C-master access to the local AHB bus,
 enabling remote monitoring, configuration, debug, or data exchange. The selection between
 normal and bridging operation modes is under software control via the core’s control
 register.

The highly flexible core offers synthesis-time and run-time configuration options, which allow
 adapting its size and behavior to the application requirements. For example, the AHB-
 master interface and the clock domains synchronizers can be removed at synthesis to
 reduce the core’s silicon footprint. During run-time, the I3C private data and I2C traffic can
 be bridged to the core’s AHB-master interface or transferred to and from the host via the
 core’s slave APB interface. Also, parameters defining the CCCs processing (e.g. own-
 address, provisional ID, acknowledge for different type CCCs), the over-I3C protocol (i.e.
 number address bytes, max number of data bytes) and the AHB-master port behavior (e.g.,
 AHB burst type & address wrapping) are all run-time configurable via the core’s registers.

The I3C-S core adheres to the industry’s best coding and verification practices to ensure trouble-free implementation in ASIC or
FPGA technologies. Technology mapping, constraining, and scan insertion are straight-forward, as the core contains no multi-cycle or
false paths and uses only rising-edge-triggered D-type flip-flops, no tri-states, an asynchronous reset line per clock domain, and clean
clock domain crossing modules. Its reliability and low risk have been proven through rigorous verification and FPGA validation.

Applications
The I3C-S core can add economical and low-power I3C data transfer capabilities to sensors, actuators, power regulators, analog
 front-ends, microcontroller peripheral devices, microcontrollers, or even FPGA devices and designs.
Implementation Results

The I3C-S can be mapped to any AMD FPGA device, provided sufficient resources are available. The following table provides sample silicon resources utilization data. Please contact CAST to get characterization data for your target configuration and technology.

<table>
<thead>
<tr>
<th>FPGA Family</th>
<th>Configuration</th>
<th>Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kintex7</td>
<td>Minimum</td>
<td>882 LUTs</td>
</tr>
<tr>
<td></td>
<td>Full, without CDC, 32x16 FIFOs</td>
<td>2,432 LUTs</td>
</tr>
<tr>
<td></td>
<td>Full, with CDC, 32x16 FIFOs</td>
<td>2,493 LUTs</td>
</tr>
<tr>
<td>Kintex UltraScale™</td>
<td>Minimum</td>
<td>897 LUTs</td>
</tr>
<tr>
<td></td>
<td>Full, without CDC, 32x16 FIFOs</td>
<td>2,280 LUTs</td>
</tr>
<tr>
<td></td>
<td>Full, with CDC, 32x16 FIFOs</td>
<td>2,473 LUTs</td>
</tr>
<tr>
<td>Kintex UltraScale+™</td>
<td>Minimum</td>
<td>897 LUTs</td>
</tr>
<tr>
<td></td>
<td>Full, without CDC, 32x16 FIFOs</td>
<td>2,280 LUTs</td>
</tr>
<tr>
<td></td>
<td>Full, with CDC, 32x16 FIFOs</td>
<td>2,473 LUTs</td>
</tr>
</tbody>
</table>

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been rigorously verified through extensive synthesis, place and route, simulation runs, with in-house and 3rd party verification. The core is silicon-proven.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms. It ships with everything required for successful implementation, including:

- Verilog RTL source code
- Post-synthesis EDIF (netlist licenses)
- Testbenches for behavioral and post-synthesis verification
- Simulation & Synthesis scripts
- Documentation

About the MIPI I3C Basic Specification

The MIPI I3C Basic specification is a subset of the MIPI I3C Specification that is publicly accessible and intended to be implementable by non-MIPI organizations under a RAND-Z license.

The Royalty-free MIPI I3C Basic provisions a multidrop two-wire serial bus operating up to 12.5MHz that provides many of the I3C protocol innovations, including in-band interrupts, dynamic address assignment and backward compatibility with I2C.

Learn more at MIPI I3C official web page.