

ZipAccel-D

GUNZIP/ZLIB/Inflate Data Decompressor



ZipAccel-D is a custom hardware implementation of a lossless data decompression engine that complies with the Inflate/Deflate, GZIP/GUNZIP, and ZLIB compression standards.

The core features fast processing, with low latency and high throughput. On average the core outputs three bytes of decompressed data per clock cycle, providing over 3Gbps on most Xilinx devices. Designers can scale the throughput further by instantiating the core multiple times to achieve throughput rates exceeding 100Gbps. The latency is in the order of a few tens of clock cycles for blocks coded with static Huffman tables, and typically less than 2,000 cycles for blocks encoded with dynamic Huffman tables.

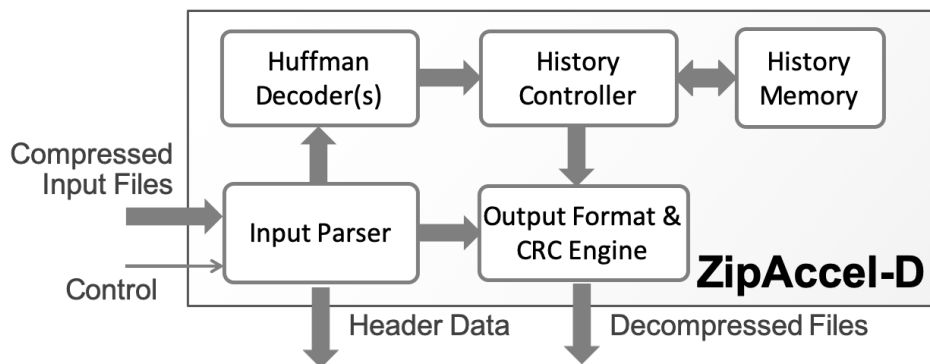
The decompression core has been designed for ease of use and integration. It operates on a standalone basis, off-loading the host CPU from the demanding task of data decompression. The core receives compressed input files and outputs decompressed files. No preprocessing of the compressed files is required, as the core parses the file headers, checks the input files for errors, and outputs the decompressed data payload. Featuring extensive error tracking and reporting errors, the core enables smooth system operation and error recovery, even in the presence of errors in the compressed input files. Furthermore, internal memories can optionally support Error Correction Codes (ECC) to simplify the achievement of Enterprise-Class reliability or functional safety requirements.

The ZipAccel-D core is a microcode-free design developed for reuse in ASIC and FPGA implementations. Streaming data, optionally bridged to AMBA AXI4-stream, interfaces ease SoC integration. Technology mapping is straightforward, as the design is scan-ready, LINT-clean, microcode-free, and uses easily replaceable, generic memory models.

Applications

The ZipAccel-D core is ideal for increasing the bandwidth of optical, wired or wireless data communication links, and for increasing the capacity of data storage in a wide range of devices such as networking interface/routing/storage equipment, data servers, or SSD drives. The core can also help reduce the power consumption and bandwidth of centralized memories (e.g. DDR) or interfaces (e.g. Ethernet, Wi-Fi) in a wide range of SoC designs.

Block Diagram



FEATURES

Compression Standards

- ZLIB (RFC-1950)
- Inflate/Deflate (RFC-1951)
- GZIP/GUNZIP (RFC-1952)

Inflate/Deflate Features

- Up to 32KB history window size
- All Deflate-block types
 - Static and dynamic Huffman-coded blocks
 - Stored Deflate blocks

High Performance & Low Latency

- Three bytes per clock average processing rate, for throughputs exceeding 3Gbps in most modern Xilinx FPGA technologies, and scalable to more than 100Gbps with multiple core instances
- Latency from 20 clock cycles for Static Huffman blocks, and typically less than 2000 cycles for Dynamic Huffman blocks

Easy to Use and Integrate

- Processor-free, standalone operation
- Extensive error catching & reporting for smooth operation and recovery in the presence of errors
 - Header syntax errors
 - CRC/Adler 32 errors
 - File size errors
 - Coding errors
 - Huffman tables errors
 - Non-correctable ECC memory errors
- Optional ECC memories
- AXI-stream or native FIFO-like data interfaces
- Microcode-free, LINT-clean, scan-ready design

Configuration Options

- Synthesis time configuration options allow fine-tuning the core's size and performance (partial list):
 - Input and output bus width
 - FIFO sizes
 - Maximum history window
 - Static-only or dynamic and static Huffman tables support

Performance and Area

The ZipAccel-D core can be mapped in any AMD FPGA device, providing sufficient resources are available. The FPGA resources requirements and throughput depend on the core's configuration. Also, the ZipAccel-D's performance can scale by using multiple core instances.

The following are sample implementation results for two configurations of the core on AMD devices. These results do not represent the smallest possible area requirements nor the highest possible clock frequency.

Family / Device	Freq. (MHz)	Logic Resources	Memory Resources	Gbps
Spartan-7 xc7s100-1	75	12,593 LUTs	23 BRAM Tiles	1.80
Kintex Ultrascale xcku085-1-c	200	14,761 LUTs	12 BRAM Tiles	4.80
Artix Ultrascale+ xcav25p-1-e	125	13,679 LUTs	14 BRAM Tiles	3.00
Kintex Ultrascale+ xcku9p-1-e	200	14,642 LUTs	12 BRAM Tiles	4.80
Versal Premium xcvp1202-2MP-e-L	200	16,791 LUTs	2 URAMs 0.5 BRAM Tile	4.80

Table 1: Implementation results for a sample configuration supporting both Dynamic and Static Huffman Tables, and a 32kB History

Family / Device	Freq. (MHz)	Logic Resources	Memory Resources	Gbps
Spartan-7 xc7s100-1	100	3,910 LUTs	9 BRAM Tiles	2.40
Kintex Ultrascale xcku085-1-c	325	4,328 LUTs	9 BRAM Tiles	7.80
Artix Ultrascale+ xcav25p-1-e	225	4,309 LUTs	8 BRAM Tiles	5.40
Kintex Ultrascale+ xcku9p-1-e	325	4,336 LUTs	8 BRAM Tiles	7.80
Versal Premium xcvp1202-2MP-e-L	300	4,364 LUTs	2 URAMs	7.20

Table 2: Implementation results for a sample configuration supporting only Static Huffman Tables, and a 32kB History

Contact CAST Sales for help defining likely configuration options and estimating implementation results for your specific system.

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has also been embedded in several commercially-shipping products and is proven in both ASIC and FPGA technologies.

The core has been verified for interoperability with a number of software applications that use GZIP, ZLIB, or Deflate compression.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms and includes everything required for successful implementation. The ASIC version includes:

- HDL (Verilog) RTL source code
- Sophisticated Test Environment
- Simulation scripts, test vectors and expected results
- Synthesis script
- Comprehensive user documentation

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Related Cores

- ZipAccel-C: GZIP/ZLIB/Deflate Data Compression Core
- GZIP-RD-XIL: GZIP & GUNZIP Accelerator Reference Design for AMD FPGAs