SHA-384/512
SHA-384 and SHA-512 Secure Hash Crypto Engine

The SHA-384/512 is a high-throughput, and compact hardware implementation of the SHA-384 and the SHA-512 cryptographic hash functions provisioned by the FIPS180-4 standard.

The core is designed for ease of use and integration and adheres to industry-best coding and verification practices. Technology mapping, and timing closure are trouble-free, as the core contains no multi-cycle or false paths, and uses only rising-edge-triggered D-type flip-flops, no tri-states, and a single-clock/reset domain. The SHA-384/512 core features a simple input and output data interface. Support for AMBA bus interfaces and integration with an external DMA are available as options.

The highly reliable SHA-384/512 has been production-proven in several ASIC and FPGAs designs.

**Block Diagram**

![Block Diagram of SHA-384/512](image)

**Applications**

The SHA-384/512 can be used in various applications for ensuring data integrity, and authenticity. Some examples are on-chip communication, electronic fund transfers, digital signatures, password storage, blockchain technology and data backup.

**Implementation Results**

The SHA-384/512 core can be mapped to any Intel® FPGA device (provided sufficient silicon resources are available). The following are sample results with all core I/Os assumed to be routed on-chip.

<table>
<thead>
<tr>
<th>Family</th>
<th>Logic</th>
<th>Memory</th>
<th>Freq. (MHz)</th>
<th>Throughput (Mbps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Agilex (-2)</td>
<td>1,872 ALMs</td>
<td>-</td>
<td>375</td>
<td>4,741</td>
</tr>
<tr>
<td>Arria 10 GX (-1)</td>
<td>1,930 ALMs</td>
<td>4 RAMB</td>
<td>250</td>
<td>3,160</td>
</tr>
</tbody>
</table>

The provided figures do not represent the higher speed or smaller area for the core. Please contact CAST to get characterization data for your target configuration and technology.

**Support**

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

**Deliverables**

The core is available in RTL (VHDL or Verilog) source code, or as a targeted FPGA netlist. Its deliverable package includes the following:

- Sophisticated self-checking HDL testbench
- C Model & test vector generator
- Sample simulation & synthesis scripts
- User documentation

**Export Permits**

This core implements encryption functions and as such it is subject to export control regulations. Export to your country may or may not require a special export license. Please contact CAST to determine what applies in your specific case.