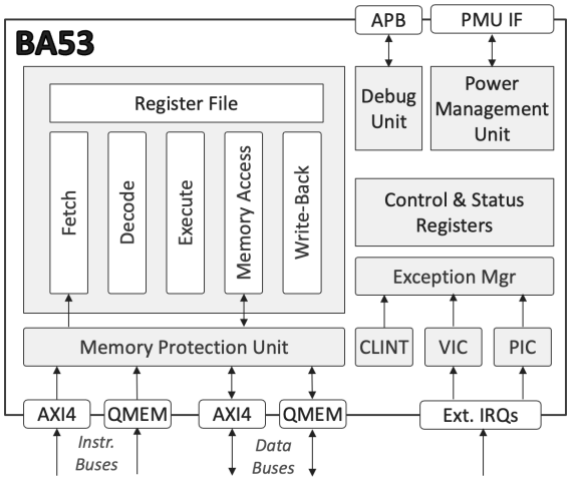
BA53

Low-Power Deeply Embedded RISC-V Processor

The BA53 is a configurable, low-power, deeply-embedded RISC-V processor IP core. It implements a single-issue, in-order, 5-stage execution pipeline, and supports the RISC-V 32-bit base integer instruction set (RV32I), or the 32-bit base embedded instructions set (RV32E).

Configuration Options for Broad Application Support

The processor core can be configured to meet different application requirements. It can optionally support user and supervisor privilege modes, as well as the ISA extensions for Compressed Instructions (C), Integer Multiplication and Division nstructions (M), Atomic Instructions (A), User-Level Interrupts (N), Control and Status Register (Zicsr), and Instruction-Fence (Zifencei). Support for the single-precision floating-point (F), double-precision floating-point (D). and Code Size Reduction (Zc) ISA extensions can also be added upon request.



Furthermore, the BA53 supports software and timer interrupts and up to 64 external interrupt lines. It features a remarkably low interrupt response time, which makes the core ideal for real time control applications.

The user can minimize the core's silicon footprint by choosing not to implement internal modules such as the machine mode internal timers and counters; the vectored interrupt controller (VIC); or the debug, power management (PMU), or memory protection (MPU) units. Finer-grained controls give users the means to further tune the processor's features and size to their specific design needs, including the number and size of memory regions for the MPU, the mapping of memory addresses to interfaces, and the width of the instruction and data buses.

Compact & Energy Efficient

Designed for low power consumption, the BA53 is compact and enables advanced power management. Under its minimal configuration, the processor size is just 30k gates. This small silicon footprint is critical for minimizing leakage currents during idle or standby modes and for reducing dynamic power consumption. The BA53 also enables dynamic clock gating or power shut-off of unused modules, and software or hardware dynamic frequency scaling of the bus and the CPU. The carefully designed and balanced pipeline allows clocking the BA53 with clock frequencies exceeding 1GHz on a 12nm technology.

Easy Integration and Low Risk

The processor core uses AMBA® AXI-4 and low-latency Quick-access Memory (QMEM) interfaces for fetching instructions and accessing data and peripherals. The debug unit connects to an external JTAG/TAP controller via an APB port.

Part of the family of processor cores available from CAST for nearly ten years and used by hundreds of customers, the BA53 IP core has been designed for easy reuse and integration. It has been rigorously verified, and is LINT-clean, scan-ready and silicon proven. It is available in Verilog source code for ASICs or FPGAs.

FEATURES

Efficient Deeply Embedded Processor

- Single-issue, in-order, 5-stage pipeline
  - 2.53 Coremarks/MHz
  - Over 1GHz in 22nm
- Small silicon footprint for lower leakage and dynamic CPU power
  - From 30k gates
- Advanced power management
  - Dynamic clock gating and unused units power shut off
  - Software- and hardware-controlled clock frequency scaling
- Harvard architecture with separate instruction and data AXI- Lite and Quick-access Memory (QMEM) buses

RISC-V Compatible

- 32-bit Base RISC-V ISA (I/E) with optional M, A, Zicsr, Zifencei, C, N, F, D, and Zc Extensions
- Supervisor, User, and Machine Modes
- Memory protection unit with a configurable number of regions
- Core Local Interrupt Controller (CLINT) for timer and software interrupts
- Programmable and/or Vectored Interrupt Controller (PIC or VIC) for up to 64 direct external interrupts

Available Pre-Integrated Platforms

- Integrate bus fabric with peripherals such as GPIO, UART, Real-Time Clock, Timers, I2C, and SPI
- Optionally customized to include memory controllers, interconnects and more from the CAST IP line

Deliverables

- Available in Verilog source-code for ASIC or FPGA
- Comprehensive Documentation
- Testbench and sample simulation scripts

Low Risk & Flexible Licensing

- Reliable vendor with an extensive track record and excellent support
  - Thousands of IP core licenses, and billions of units shipped with IP from CAST since 1993
  - Experienced and responsive support team with a 24/7 culture
- Industry-standard licensing terms with royalty-free options

Applications

The royalty-free, energy-efficient BA53 processor can be employed as an effective replacement for existing 8-bit and 16-bit microcontrollers, or used as secondary, housekeeping, or peripheral controller processor in complex SoC designs. It is suitable for a wide range of deeply embedded applications such as mixed-signal embedded processing (e.g. SERDES control), wireless communication ICs (e.g. Bluetooth, Zigbee, or GPS), and industrial microcontrollers.

Software Development

The BA53 can be used with RISC-V compatible toolchains, libraries, and IDEs. However, BA53 processor users can also benefit from using BeyondStudio™, an Eclipse-based Integrated Development Environment (IDE) that combines an Instruction level simulator and a GNU cross-compiling toolchain. Employed by numerous BAx processor users for over a decade, BeyondStudio has evolved to become a complete and highly featured IDE.

Reference designs on FPGA development boards are available to ease evaluations and accelerate code development. Contact CAST Sales for more information.

Support and Services

The core as delivered is warranted against defects for 90 days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

IP Integration Services are also available to help minimize time to market for BA53-based systems. The processor core can be delivered pre-integrated with bus infrastructure cores, typical microcontroller peripherals, memory controllers, and interconnect IP cores. Contact CAST Sales for details.

Deliverables

The core is available in synthesizable Verilog source code. It deliverable package includes everything required for successful implementation: extensive documentation, a testbench, a sample SoC design, and sample synthesis and simulation scripts.