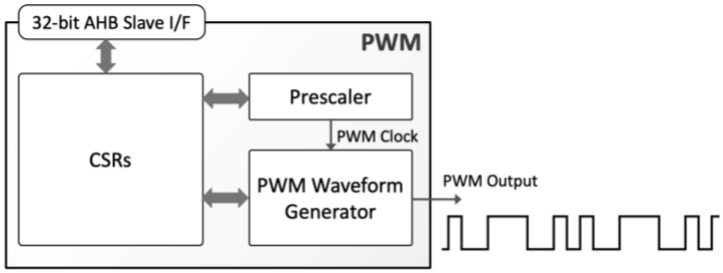
PWM

Pulse Width Modulator

The PWM IP core implements a compact and highly flexible Pulse Width Modulator. The core generates a repeated pattern of pulse trains of run-time configurable period and duty cycle. Those pulse trains can be used in a wide variety of applications including but not limited to motor control and LED dimming. They can also be filtered with a lowpass filter to implement Digital to Analog Converters (DAC).

The core is designed for ease of use and integration and adheres to the industry's best-standards coding and verification practices. It provides access to its control and status registers via a 32-bit AMBA™ AHB or Wishbone slave port. APB, AXI4-Lite, or other interfaces can be made available on request. Technology mapping, timing closure, and scan insertion are trouble-free, as the core contains no multi-cycle or false paths and uses only rising-edge-triggered D-type flip-flops, and no tri-states.

Block Diagram



FEATURES

Advanced PWM Features

- Run-time programmable PWM pattern
  - Limits long high or low times
  - Essential for efficient DAC implementations
- Fine control of PWM period
  - A 16-bit register value defines the length of the PWM period in terms of PWM clock cycles
  - PWM clock derived using a fractional prescaler with 16-bit denominator and 16-bit numerator
- Updated PWM parameters applied either immediately or on the next PWM period.

Interfaces

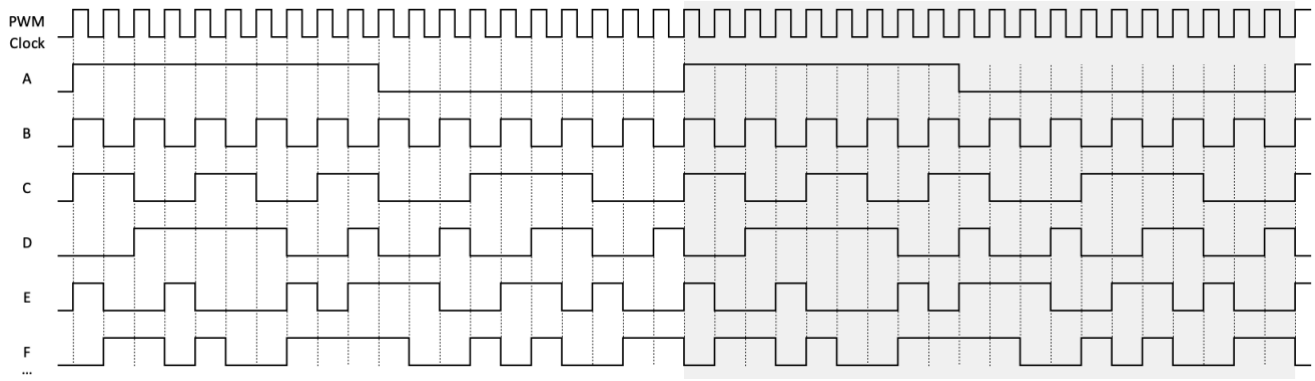
- 32-bit AHB or Wishbone Slave for CSR access
  - APB or AXI4-Lite interface available on request

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Integration Test-Bench
- Simulation & synthesis scripts
- Comprehensive user documentation

Functional Description

The pulse train generation is timed with the PWM clock. A fractional pre-scaler with a programmable 16-bit denominator and 16-bit numerator allows generation of the PWM clock with high accuracy. Great flexibility is also provided in the setting of the period of the PWM pattern, which is also run-time programmable and can take values in the range of 2 to 2^{16} PWM clock cycles. What sets this IP core apart from most conventional PWM controllers is that it allows the pulse train pattern to be configurable. This avoids long high or low times, which are problematic in several use cases. For example, the long high or low times can limit the bandwidth and accuracy of a DAC implemented by filtering the PWM pulse train. The following picture illustrates some of the possible output PWM waveforms with a period of 20 cycles, and a duty cycle of 50%. Note that conventional PWM controllers are only capable of producing waveform A.



Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has also been embedded in several products and is proven in both ASIC and FPGA technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.