# TSN-EP

## TSN Ethernet Endpoint Controller

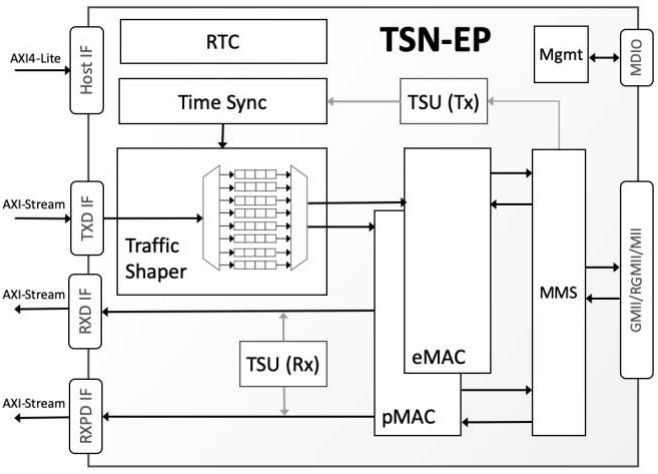
The TSN-EP implements a configurable controller meant to ease the implementation of endpoints for networks complying to the Time Sensitive Networking (TSN) standards. It integrates hardware stacks for timing synchronization (IEEE 802.1AS-2020) and traffic shaping (IEEE 802.1Qav and 802.1Qbv), frame-preemption (IEEE 802.1Qbu and IEEE 802.3br) and a low-latency Ethernet MAC. Enhanced reliability features can also be supported, using the optional hardware modules for Frame Replication and Elimination for Reliability (IEEE 802.1CB) and Per-Stream Filtering and Policing (IEEE 802.1Qci).

The controller core is designed to enable high-precision timing synchronization and flexible yet accurate traffic scheduling. Requiring minimal software assistance for its initialization, it features extremely low and deterministic ingress and egress latencies and simplifies the development of time-aware applications. While operating autonomously, the TSN-EP provides the system with timing information (timestamps, alarms, etc.) that is typically required for the operation of a TSN network endpoint device. Furthermore, it allows the system to define and tune in real time the traffic shaping parameters according to an application's requirements.

The TSN-EP uses standard AMBA® interfaces to ease integration. Its configuration and status registers are accessible via a 32-bit-wide APB bus, and packet data are input and output via 32-bit-wide AXI-Streaming buses. To further expedite and ease the implementation of customer applications, CAST offers software stacks supporting higher-layer protocols, such as IEEE 802.1Qcc, IEEE 802.1Qca and SNMP, as well as hardware integration and software porting services.

The TSN-EP is designed with industry best practices and is available in synthesizable RTL (Verilog 2001) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

## Block Diagram




## Applications

The TSN-EP is suitable for the implementation of sources of traffic and bridges for TSN Ethernet networks requiring robust, low-latency, and deterministic communication. Such networks are used in automotive, industrial control, and aerospace applications.

## FEATURES

### TSN Ethernet Endpoint

- One Ethernet port & one host processor port
- Suitable for star-topology networks
- 10/100/1000 Mbps Ethernet

### Time Synchronization

- Implements IEEE 802.1AS-2020
- Grandmaster or Slave functionality
- Highly accurate synchronization. Accuracy is typically in the order of a few tens ns.
- Provides the system with timestamps, periodic event triggers, and alarms

### Traffic Shaping

- Implements Traffic Scheduling as per IEEE 802.1Qav and IEEE 802.1Qbv
- Implements Frame Preemption as per IEEE 802.1Qbu and IEEE 802.3br
- Supports up to 8 traffic classes, as per VLAN (IEEE 802.1Q)
- Enables bandwidth reservation and allocation per traffic class, and deterministic, low-latency, low-jitter communication for all traffic classes

### Optional TSN Protocols

- Frame Replication and Elimination (IEEE 802.1CB) and Per-Stream Filtering and Policing (IEEE 802.1Qci) optionally implemented in hardware
- Path Control and Reservation per IEEE 802.1Qca, and Enhancements to Stream Reservation Protocol per EEE 802.1Qcc are optionally implemented in software

### Easy System Integration

- AMBA/AXI4 Interfaces
  - 32-bit APB for control/status registers
  - 32-bit AXI4-Stream for packet data
- MII, GMII and RGMIII Ethernet PHY interface
- Complete reference designs available, including sample application software
- Requires minimal host assistance for its initialization

### Verification IP

- The TSN-VIP Ethernet Verification IP package is available for this core

## Implementation Results

The TSN-EP can be mapped to any Intel® FPGA device (provided sufficient silicon resources are available). The FPGA resources requirements depend on the core configuration. The following are sample results for a typical core configuration. Please contact CAST to get characterization data for your target configuration and technology.

| Family/Device | Config.* | Logic | Memory |
|---|---|---|---|
| **Cyclone V** 5CSXFC6D6F31C6 | 8 Traffic Queues 1k Queue Depth RTC, Traffic Shaper, Preemption | 5,530 ALMs | 389,320 bits |

*Partial list of configuration parameters

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The TSN-EP has been rigorously verified, hardware-validated, and tested in real-life environments.

It has also been tested and verified at TSN interoperability plugfests organized by the Labs Network Industry 4.0 (LNI 4.0) association and the Industrial Internet Consortium (IIC).

The TSN-VIP TSN Ethernet Verification IP package is also available, to help test the TSN-EP or an SoC containing it.

## Deliverables

The core includes everything required for successful implementation:

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation
- Lightweight PTP stack and device driver for FreeRTOS, easily portable to any other RTOS.

Customers may optionally choose to license the TSN-EP core pre-integrated with a deeply embedded processor running the PTP stack.

## Related Products

The core is a member of CAST's family of automotive interface products that includes:

- TSN-SE TSN Ethernet Switched Endpoint IP core
- TSN-SW: TSN Ethernet Switch IP Core
- TSN-VIP TSN Ethernet Verification IP
- LLEMAC-1G Low-Latency 10/100/1000 Ethernet MAC IP core
- CAN 2.0/CAN FD/CAN XL Controller IP core
- CAN 2.0/CAN-FD Verification IP
- LIN 2.2/2.1/2.0 Master/Slave Controller IP core
- SENT / SAE J2716 Transmitter/Receiver Controller IP core