TCP/IP Hardware Stack IP Core now Available from CAST

Complete, efficient, autonomous, and highly configurable core implements the entire TCP stack in scalable hardware for ASICs and FPGAs

Woodcliff Lake, New Jersey — October 13, 2022 — Semiconductor intellectual property provider CAST today announced the immediate availability of a TCP/IP Stack core that connects a system to the Internet and manages communication using the TCP protocol while requiring no assistance from the system's processor.

The new **TCPIP-1G/10G Hardware Stack** IP core implements a hardware stack for the TCP/IP protocol that transmits or receives data over Ethernet at speeds of 10/100/1000Mbps, 2.5Gbps, and 10Gbps. Going beyond many TCP/IP "offload engines," the new CAST core is:

- Complete — It can implement the entire stack in hardware: IP, VLAN, ARP, ICMP (ping), DHCP client, UDP stack, and TCP.
- Autonomous — It networks and exchanges data without requiring assistance from—or even the presence of—a system processor (beyond initialization).
- Efficient — It uses network bandwidth better than basic transmit/receive cores by including advanced flow and congestion control algorithms that minimize data loss, retransmission, and congestion.
- Configurable — It can be optimized for a range of applications, from edge devices like sensors that periodically transmit data and need minimum power and latency up to complex data-server network interface cards able to efficiently handle thousands of sessions.
- Portable — It offers the flexibility to implement the stack in any ASIC or FPGA technology, helping projects remain on schedule despite today's uncertainties about device manufacturing and delivery timelines.

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"We've worked with networking IP users for years and learned from the TCP/IP stacks already available to engineer what we believe is a better core that can satisfy the requirements of nearly any system needing TCP/IP communication," said Andreas Emeretlis, hardware design engineer for CAST.

The configurable options of the TCPIP core include setting the maximum number of TCP sessions from one to 32,768; enabling or disabling the built-in DHCP client or UDP stack; and handling data packets in cut-through or store-and-forward mode. For the latter, cut-through mode immediately passes data to the system for the lowest possible latency, while store-and-forward mode only sends verified data packets guaranteed to be in order, at the expense of somewhat greater latency and silicon area.

Integration of the TCPIP core is simplified through its use of standard AMBA interfaces for connections to external memory and the host system. It works with any standard Ethernet MAC core (including CAST's), and it can utilize any type of external memory.

The TCPIP-1G/10G Hardware Stack IP Core is available now in synthesizable RTL for ASICs or as an FPGA netlist for Intel, Lattice, Microsemi, or Xilinx devices. Sample designs integrating the TCPIP core with third-party or CAST's Ethernet MAC and/or memory controllers are available; email CAST Sales for more information.

This is the first of a series of TCP/IP Stack cores CAST plans to release, with 40G and 100G capable cores coming next year. All benefit from a decade of CAST successfully delivering UDP/IP cores, the expertise of CAST's engineering team in both networking and IP reusability, and the company's industry-leading IP quality and customer support services.

About CAST

Computer Aided Software Technologies, Inc. (CAST) is a silicon IP provider founded in 1993. CAST's ASIC and FPGA IP product line includes microcontrollers and processors; compression engines for data, images, and video; interfaces for automotive, aerospace, and other applications; various common peripheral devices; and comprehensive SoC security modules. Learn more by visiting www.cast-inc.com.

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