CSENT
SENT/SAE J2716 Controller

The CSENT core implements a controller for the Single Edge Nibble Transmission (SENT) protocol. It complies with the SAE J2716 standard and is capable of driving pulses to trigger synchronous Sensor type. It can be used for conveying data from one or multiple sensors to a centralized controller using a single SENT line.

The CSENT core can be configured as a Transmitter and/or as a Receiver, and therefore it is suitable for adding a SENT interface to devices transmitting sensor data or controllers receiving sensor data. It provides access to its control, status, and data registers through a 32-bit APB bus interface, and a comprehensive set of interrupt signals facilitates interrupt-based operation. The core allows for Transmitter operation without requiring any external programming or control. The reset values for all its control registers are defined at synthesis time, and at run time the system only needs to write sensor data to the core.

The CSENT core is designed with industry best practices. The core contains no latches or tri-states, and is fully synchronous with a single clock domain. The core is available in Verilog RTL or as targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

Applications
The CSENT core is suitable for designing low-cost digital automotive sensors and automotive controller units.

Size and Performance
The core can be mapped to any ASIC technology and any FPGA device from Intel/Altera, are sample implementation results, which do not represent the highest speed or smallest area area for the implementation of the FIFOs.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Target Technology</th>
<th>Area</th>
<th>Fmax</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx and Rx</td>
<td>TSMC 28hpm</td>
<td>2,410 um² / 4,850 Gates</td>
<td>1,000 MHz</td>
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<tr>
<td></td>
<td>Xilinx, Kintex-7</td>
<td>781 LUTs</td>
<td>361 MHz</td>
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<tr>
<td></td>
<td>Altera, Stratix V</td>
<td>570 ALMs</td>
<td>315 MHz</td>
</tr>
<tr>
<td>Tx only</td>
<td>TSMC 28hpm</td>
<td>1,152 um² / 2,300 Gates</td>
<td>1,000 MHz</td>
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<tr>
<td></td>
<td>Xilinx, Kintex-7</td>
<td>430 LUTs</td>
<td>358 MHz</td>
</tr>
<tr>
<td></td>
<td>Altera, Stratix V</td>
<td>275 ALMs</td>
<td>339 MHz</td>
</tr>
</tbody>
</table>

FEATURES
SENT/SAE J2716 Receiver & Transmitter
- Fast and Slow Channel Transmit or Receive
- CRC generation for Transmitter, and CRC checking for Receiver
- All types of SENT Frames
  - Programmable data length (4 to 24 bits) for Fast Channel Frames
  - Short (8-bit data) and Enhanced (12- or 16-bit data) Message Formats for Slow Channel
- Optional Pause Pulse with programmable length
- Supports inverted SENT protocol

Trigger Pulse for Synchronous Sensors
- Allows up to four sensors (transmitters) to use the same physical SENT connection
- Programmable master trigger pulse length

Ease of Integration
- 32-bit APB interface, and comprehensive set of interrupts
- Programmable 4-bit clock divider and high precision 16-bit clock pre-scale
- Receive and Transmit FIFO of configurable size for Fast Channel data
- Run-time programmable configuration registers
- Synthesis-time defined reset values for all registers, enables data transmit without control from host processor
- LINT-clean, single-clock domain, scan-ready design

Deliverables
- Targeted netlist
- Testbench
- Sample synthesis and simulation scripts
- Documentation