

# TSN-SW

## Multiport TSN Ethernet Switch



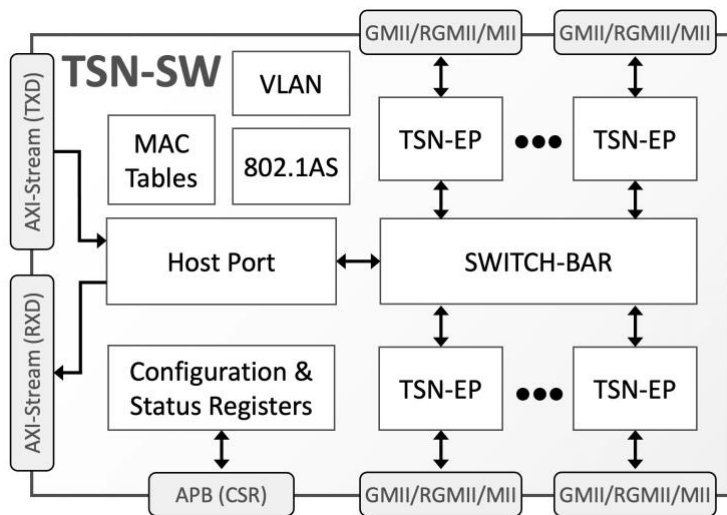
The TSN-SW implements a highly flexible, low-latency, multiport TSN Ethernet switch. It supports Ethernet bridging according to the IEEE 802.1Q-2018 standard and implements the essential TSN timing synchronization and traffic-shaping protocols (i.e. IEEE 802.1as, 802.1Qav, 802.1Qbv, 802.1Qbu, 802.1br and optionally 802.1Qci, and 802.1CB). Featuring a configurable number of ports, the Layer-2 switch operates in cut-through mode at wire speed and can provide sub-microsecond port-to-port latency. The core is hence suitable for applications with demanding real-time requirements.

The TSN-SW operates efficiently under different usage scenarios and is highly configurable. Users can configure key factors via the core's control registers: the mapping of VLAN priority levels to TSN traffic classes, the traffic scheduling and preemption parameters, the treatment of special frames (i.e. broadcast, unknown, & internal), as well as the VLAN ID and MAC lookup tables used for frame forwarding and filtering. The host system can also switch the mode of operation of each individual port from cut-through to store-and-forward to eliminate the propagation of bad frames at the cost of increased latency. The core otherwise operates autonomously and only requires software assistance at runtime for correct time synchronization; a lightweight ptp/802.1AS software stack comes with the core for that purpose.

The TSN-SW uses standard AMBA® interfaces to ease integration. Its control and status registers are accessible via a 32-bit-wide APB bus, and packet data can be exchanged with the host system via AXI-Streaming interfaces with 32-bit data buses.

The TSN-SW is designed with industry best practices and is available in synthesizable RTL (Verilog 2001) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample synthesis and simulation scripts, an extensive testbench, and comprehensive documentation.

### Block Diagram



### Applications

The TSN-SW is suitable for implementing TSN Ethernet Endpoints in daisy-chained networks (e.g. ring topologies) requiring robust, low-latency, and deterministic communication. Such networks are used in automotive, industrial control, medical, and aerospace applications.

### FEATURES

#### Low-Latency & Flexible Ethernet Switch

- Configurable number of 3 to 15 full-duplex Ethernet ports plus one internal port
  - More than 15 Ethernet ports available upon request
- Layer-2, cut-through switching at wire speed
  - The store-and-forward mode can be enabled per port at run time
- Sub-microsecond port-to-port latency, in cut-through mode
- 10/100/1000 Mbps Ethernet speeds (2.5/10+ Gbps on request)
- 802.1Q-2018 Tagged VLAN support
- Port-based VLAN
- Configurable VLAN-PCP to TSN-queue mapping (QoS by PCP)
- Flexible VLAN and MAC forwarding & filtering
- Configurable VLAN-ID & MAC lookup table for dynamic and static entries
- Automatic aging table
- Untagged ports support
- Port Statistics
- Port mirroring

#### TSN Features

- Ready for IEEE 802.1as (lightweight software stack available)
- Traffic shaping per IEEE 802.1Qav & IEEE 802.1Qbv with eight TSN-Queues
- Frame preemption per IEEE 802.1Qbu and IEEE 802.3br
- Frame Replication and Elimination for Redundancy per IEEE 802.1CB
- Per-Stream Filtering and Policing (PSFP) per IEEE 802.1Qci

#### Easy System Integration

- AMBA® SoC Interfaces
  - 32-bit APB control/status interface
  - 32-bit AXI4-Stream for packet data
- MII, GMII or RGMII, and MDIO Ethernet PHY interface per port
- Requires minimal host assistance for initialization and operation
- Provides a wide range of statistics via optionally instantiated counters
- Complete reference designs available, including lightweight PTP stack sample application software

## Implementation Results

The TSN-SW can be mapped to any Intel® FPGA device (provided sufficient silicon resources are available). The FPGA resources requirements depend on the core configuration. The following are sample results for a typical core configuration. Please contact CAST to get characterization data for your target configuration and technology.

Family/Device	Config.*	ALMs	Memory Mbits
<b>Cyclone V</b> 5CSEBA6U19C6	64 Lookup Entries 4kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth No Frame Preemption	17,692	0.83
<b>Cyclone V</b> 5CSEBA6U19C6	126 Lookup Entries 4kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth Frame Preemption	26,838	1.62
<b>Cyclone V</b> 5CSEBA6U19C6	512 Lookup Entries 4kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth Frame Preemption	33,306	2.60

\*Partial list of configuration parameters

## Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

## Verification

The TSN-SW has been rigorously verified, hardware-validated, and tested in real-life environments.

It has also been tested and verified at TSN interoperability plugfests organized by the Labs Network Industry 4.0 (LNI 4.0) association and the Industrial Internet Consortium (IIC).

## Deliverables

The core includes everything required for successful implementation:

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation
- Lightweight PTP stack, easily portable to any other RTOS

## Related Products

The core is a member of CAST's family of automotive interface products that includes:

- TSN-EP TSN Ethernet Endpoint IP Core
- TSN-SE: TSN Ethernet Switched Endpoint IP Core
- TSN-VIP TSN Ethernet Verification IP
- LLEMAC-1G Low-Latency 10/100/1000 Ethernet MAC IP core
- CAN 2.0/CAN FD/CAN XL Controller IP core
- CAN 2.0/CAN-FD Verification IP
- LIN 2.2/2.1/2.0 Master/Slave Controller IP core
- SENT/SAE J2716 Transmitter/Receiver Controller IP core