

# QOIE

## QOI Lossless Image Compression Encoder

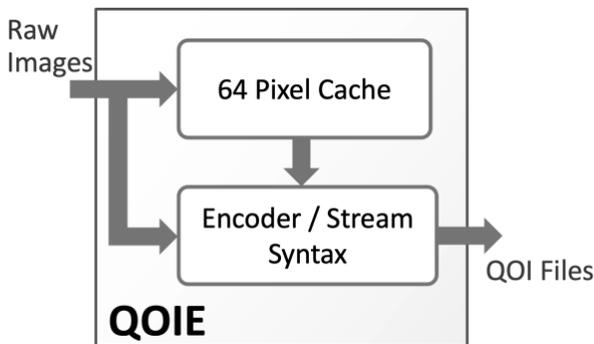
The QOIE Core is an encoder that implements a highly efficient, low-power, lossless image compression engine compliant with the Quite OK Image format (QOI) specification, version 1.0.

The QOI algorithm compresses RGB or RGBA images with 8 bits per color without any loss. It has a compression efficiency close to that of PNG compression, but with a fraction of the computational complexity.

Capitalizing on the simplicity of the QOI algorithm, the QOIE encoder core can compress images at a very high speed and with minimal silicon resources. The core occupies approximately 15,000 equivalent NAND2 gates and can process one pixel per clock cycle. A single core instance can compress images at rates sufficient for UHD 4k30 video even in low-end FPGAs, 4k60 in mid-range FPGAs, and 8k30 or 60 in modern ASIC technologies.

The core is designed for ease of use and integration and adheres to coding and verification best practices. It requires no assistance from a host processor and uses simple handshake interfaces for input and output data. Technology mapping, timing closure, and scan insertion are trouble-free, as the core contains no multi-cycle or false paths, and uses only rising-edge-triggered D-type flip-flops, no tri-states, and a single-clock/reset domain. Its reliability and low risk have been proven through rigorous verification and FPGA validation.

### Block Diagram



### Applications

Numerous applications can benefit from the tiny silicon footprint and ultra-low-power consumption of the QOI compression and decompression cores CAST offers. Typical uses include frame buffer compression for video processing SoCs; graphic elements or display buffer compression; and image storage and transmission for medical, aerospace, and other systems.

### Sample Implementation Results

The QOIE is a digital core and can be mapped to any Xilinx family or device (provided sufficient resources are available). The following are sample implementation results for Xilinx devices. These sample results do not represent the minimum area or the fastest clock speed for the QOIE core. Please contact CAST to get accurate characterization for your target device and throughput requirements.

Target Technology	Area (um <sup>2</sup> )	Eq. Gates	Freq. (MHz) / Mpixels/s
TSMC 28nm HPC tsmc28hpc-sc9-c35-ss-svt-125c	7,702	15,281	2,000
	6,953	13,995	1,000
TSMC 16nm tsmc16-sc7-svt-c16-ssgnp-125c	2,788	16,133	2,000
	2,747	15,897	1,000

### FEATURES

#### QOI Image Format

- Lossless Image Compression
- Supports RGB and RGBA, 8-bit per color images
- Compression performance similar to that of PNG with a fraction of the computational complexity

#### QOIE IP Core

- QOI compression with a compact and high-throughput hardware encoder
- Outputs raw header-less QOI files
  - Optional QOI header generation
- Supports RGB images
  - RGBA support can be added on request

#### High-Throughput

- 1 pixel per clock-cycle throughput
- A single core can process UHD 4k60 in mid-range FPGAs, and 8k60 on modern ASIC technologies

#### Compact and Low-Power

- Approximately 15,000 gates

#### Deliverables

- VHDL or Verilog RTL source code or targeted FPGA netlist
  - Verilog can be made available on request
- C-model for test vectors generation
- Integration Test-Bench
- Simulation & synthesis scripts
- User documentation

