HSDLC
HDLC & SDLC Protocol Controller

The HSDLC IP core implements a controller for the High-Level Data Link Control (HDLC) and the Synchronous Data Link Control (SDLC) protocols. It is based on the Intel® 8XC152 Global Serial Channel (GSC) working in SDLC mode, and adds features to support HDLC or proprietary frame transmission under host processor control.

The core operates as a peripheral to a host processor, and is easy to integrate with both modern and legacy processors. Control and status registers are accessible via an APB or a generic 80C51-like bus interface, and a comprehensive set of interrupt signals facilitates interrupt-based operation.

The controller’s great flexibility enables a variety of serial link setups. It provides two independent interfaces, one for transmitting and one for receiving data. Both interfaces provide control signals for the link drivers to support both full- and half-duplex operation. The controller can be programmed to use hardware flow control signals (RTSn/CTSn) and it can also detect collisions. The baud rate is programmable and limited only by the link drivers and the core’s clock frequency. The core derives the receive clock from the received serial data, or uses an externally provided receive clock.

The HSDLC is available in two versions: Normal, and Safety-Enhanced. The Safety-Enhanced version implements triple-modular redundancy (TMR) to provide full immunity to single-bit upsets and errors and complies to Design Assurance, Level A (DAL-A) of the DO-254 standard.

The HSDLC controller core is designed for reuse and is rigorously verified and scan-ready. Although designed to manage serial links, the core contains no latches or tri-states, and is fully synchronous with a single clock domain. The core is available in Verilog RTL or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

Applications
The HSDLC controller core can be used in telecommunication equipment supporting HDLC-based protocols such as X.25 or ISDN-D. It can also be used to implement serial interfaces between processors and peripherals.

Block Diagram
Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

HSDLC core reference designs have been evaluated in a variety of technologies. The following table provides sample performance and resource utilization data. Please contact CAST to get characterization data for your target configuration and technology.

<table>
<thead>
<tr>
<th>Supported Family / Device</th>
<th>Logic</th>
<th>Memory Bits</th>
<th>Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone-V 5CEBA9F31C7</td>
<td>412 ALMs</td>
<td>0</td>
<td>162</td>
</tr>
<tr>
<td>Arria-V 5AGXBB3D4F35C4</td>
<td>414 ALMs</td>
<td>0</td>
<td>202</td>
</tr>
<tr>
<td>Arria10 10A5057K2F35I2LG</td>
<td>420 ALMs</td>
<td>0</td>
<td>327</td>
</tr>
<tr>
<td>Max10 10M50DAF484C6GES</td>
<td>836 LEs</td>
<td>0</td>
<td>136</td>
</tr>
</tbody>
</table>

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts and comprehensive user documentation.

The deliverables for the safety-enhanced version include a complete DO-254/DAL-A Certification Data Package.