H265-MP-D

HEVC/H.265 Main Profile Video Decoder

The H265-MP-D IP core implements a hardware video decoder for the High Efficiency Video Coding (HEVC) compression standard. The core complies with the Monochrome, Main, Main 10, and optionally the Monochrome 12, Main 4:2:2-10, and Main 4:2:2 12 profiles of the standard (ITU-T H.265 | ISO/IEC 23008-2).

The video decoder is designed for straightforward, trouble-free SoC integration. It operates on a stand-alone basis such that decoding proceeds without any assistance or input from the host processor.

The core features streaming-capable AMBA® AXI-S interfaces for the stream and decoded pixel data. A standard AXI4-lite system bus interface gives the host real-time control and status access. An AXI4 memory interface for reading the incoming compressed video and storing the resulting decompressed video is independent of memory type—supporting SRAM, SDRAM, or DDRAM—and tolerant to the large delays and latencies typically present on a shared bus architecture.

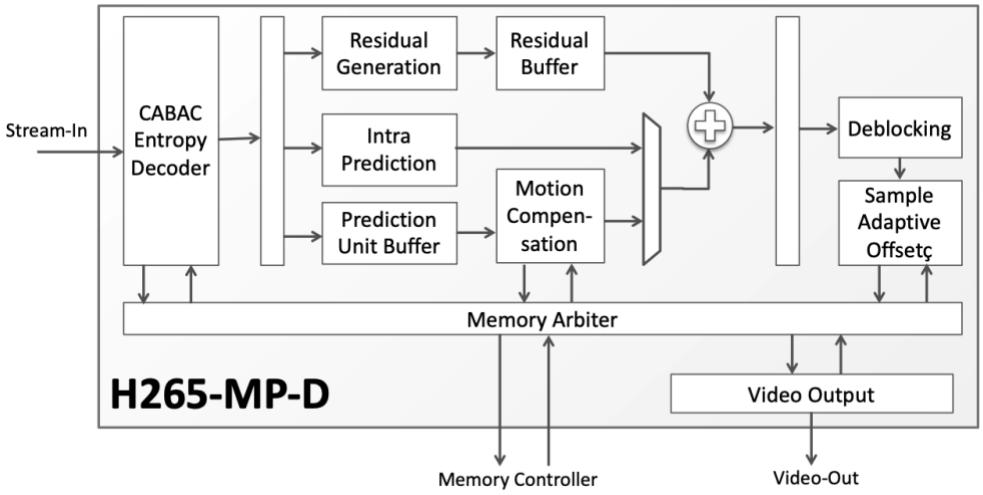
The H265-MP-D is a custom hardware accelerator and uses local memories that maximize data reuse and minimize external memory bandwidth, so its power consumption and clock frequency requirements are much lower than any software or hybrid software/hardware decoder implementation.

The H265-MP-D is a microcode-free design developed for reuse in ASIC and FPGA implementations. The design is scan-ready using strictly synchronous with positive-edge clocking and no internal tri-states. The core has been rigorously verified using Fraunhofer's reference streams and is FPGA proven.

Applications

The H265-MP-D decoder core's real-time performance and low-power operation makes it an excellent choice for 4K/UHD video broadcasting and streaming applications.

Block Diagram



FEATURES

Profiles

- Monochrome, Main, Main-10—and optionally the Monochrome 12, Main 4:2:2 10, and Main 4:2:2 12—profiles of ITU-T H.265 | ISO/IEC 23008-2

Performance

- 1080p60 and 4k/UHD@30 in FPGAs
- 4K/UHD@60 on high–end FPGAs and ASICs

Video Formats

- 4:0:0 (Monochrome), 4:2:0, and optionally 4:2:2
- 8, 10, and optionally 12 bits per color
- Maximum resolution and frame rate depend on target technology:
  - Full HD (1080p60), and UHD (4K@25) in FPGAs
  - 4K/UHD@60fps in modern ASIC nodes

Ease of Use

- Full hardwired implementation: standalone, processor-free operation
- Streaming Interfaces, and Avalon or AMBA AXI interfaces

Low Power

- Hardwired implementation with application-specific local memories: runs at lower clock frequencies and consumes less power than any software or semi-custom decoder

Deliverables

- RTL source code or targeted FPGA netlist
- Test bench
- Sample simulation and synthesis script
- Extensive documentation

Verification

Standard compliance verified with Fraunhofer HEVC Bit-stream Test Suite, and a large collection of HEVC content

www.cast-inc.com • info@cast-inc.com • tel +1 201.391.8300

Sourced from Fraunhofer HHI

Functional Description

The core is fully compliant with the HEVC Monochrome, Main, and Main 10 profiles, and optionally with the HEVC Monochrome 12, Main 4:2:2 10, and Main 4:2:2 12 profiles.

The most important coding features and tool-support offered by the core are as follows:

- CABAC is used for entropy decoding.
- Coding Tree Units (CTUs) are 64x64, 32x32, and 16x16 pixels.
- Coding Units (CUs) are 64x64, 16x16, and 8x8 pixels.
- Prediction Units (PUs) are 64x64, 32x32, 16x16, 8x8, and 4x4 pixels.
- Transformation Units (TUs) are 32x32, 16x16, 8x8 and 4x4 pixels.
- 33 directional prediction modes as well as planar and the DC mode,
- PCM mode and predictive lossless coding,
- Motion compensation with quarter-sample accuracy for all prediction unit sizes,
- Motion compensation with bi-prediction,
- Up to 16 reference frames,
- Two in-loop filters: Deblocking (DBF) and Sample Adaptive Offset (SAO).

The H265-MP-D implements a CTU pipeline with four stages: entropy decoding, residual/predictor processing, loop filtering, and SAO processing. The stages are decoupled via double buffers containing completed and currently processed CTUs. The video output unit is decoupled from the decoder pipeline via a frame buffer located in the external memory.

Resource Utilization and Performance

The H265-MP-D can be mapped to any Intel® FPGA device provided sufficient silicon resources are available. The following table indicates Xilinx families that do provide sufficient resources, and provide sample implementation data.

Config.	Performance			FPGA Resources[3]	
	Stratix® V	Arria® V	Arria® 10	ALMs	Mem. Bits/ DSPs
Minimal[1]	1080p60	720p50	1080p50	130k	2.8M/730
Full[2]	4kUHD@30	1080p30	4kUHD@25	150k	9.2M/730

1: 4:2:0, 8-bit, No long term prediction, no PCM, No Tiles support, No WPP
2: All coding tools, all supported video formats and profiles
3: Exact resource requirements depend on target device, synthesis options and megafunction configuration

Note that these sample implementation figures do not necessarily represent the highest performance or smallest area possible for the megafunction.

Please *contact CAST* to discuss resource utilization and performance for your preferred device(s).

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in synthesizable VHDL and FPGA netlist forms. It provides everything required for successful implementation, including a sophisticated self-checking testbench, simulation scripts, test vectors, and expected results, synthesis scripts and comprehensive user documentation