CAN-CTRL

CAN 2.0, CAN FD, & CAN XL Bus Controller

Implements a CAN bus controller that performs serial communication according to the CAN 2.0, CAN FD, and CAN XL specifications. It supports the original Bosch protocol and ISO specifications as defined in ISO 11898—including time-triggered operation (TTCAN) as specified in ISO 11898-4—and is also optimized to support the popular AUTOSAR and SAE J1939 specifications.

The CAN protocol uses a multi-master bus configuration for the transfer of frames between nodes of the network and manages error handling with no burden on the host processor. The core enables the user to set up economic and reliable links between various components. It appears as a memory-mapped I/O device to the host processor, which accesses the CAN core to control the transmission or reception of frames.

The CAN-CTRL core is easy to use and integrate, featuring programmable interrupts, data and baud rates; a configurable number of independently programmable acceptance filters; and a generic 32-bit or 8-bit processor interface or optionally a 32-bit AMBA APB, AHB-Lite, Wishbone, or Avalon-MM interface. It implements a flexible buffering scheme, allowing fine-tuning of the core size to satisfy the requirements of each specific application.

The number of receive buffers is synthesis-time configurable. Two types of transmit buffers are implemented: a high-priority primary transmit buffer (PTB) and a lower-priority secondary transmit buffer (STB). The PTB can store one message, while the number of included buffer slots for the STB is synthesis-time configurable. The transmit buffer can operate in FIFO or priority mode.

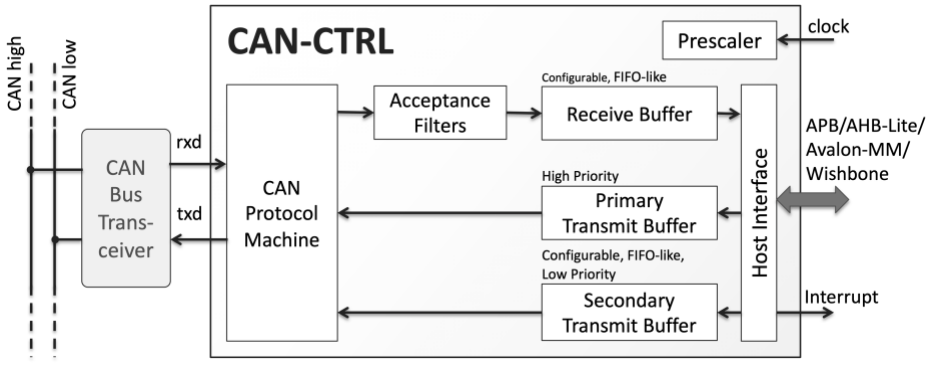
The core implements functionality similar to the Philips SJA1000 working with its PeliCAN mode extensions, providing error analysis, diagnosis, system maintenance, and optimization features.

The CAN bus controller comes in three variants: 2.0, FD, and XL. The 2.0 variant supports only the CAN 2.0 specification, the FD variant adds support for CAN FD, and the XL variant supports the CAN 2.0, CAN FD, and CAN XL standards. Each of the three core variants is available in two versions: Standard, and Safety-Enhanced. The Safety-Enhanced version implements ECC for SRAMs protection and uses spatial redundancy for protecting the inner logic of the core. The Safety-Enhanced versions are certified as *ISO-26262 ASIL-D Ready*.

Applications

The CAN-CTRL core can be integrated in devices that use CAN or higher-layer, CAN-based communication protocols. In addition to traditional automotive applications, such devices are used in industrial (e.g. CANopen and DeviceNet protocols), aviation (e,g. ARINC-825 and CAN aerospace protocols), marine (e.g. NMEA 2000 protocol) and other applications.

Block Diagram



FEATURES

CAN Specifications Support

- CAN 2.0 & CAN-FD (ISO 11898-1.2015, plus earlier ISO and Bosch specifications)
- CAN XL (CiA 610-1 specification)
- TTCAN (ISO 11898-4 level 1)
- Optimized for AUTOSAR and SAE J1939

Enhanced Functionality

- Error Analysis features enabling diagnostics, system maintenance, and system optimization:
  - Last error type
  - Arbitration lost position
  - Error Warning Limit
- Listen-Only Mode enables CAN bus traffic analysis and automatic bit-rate detection
- Loop back mode for self-testing
- Time-stamping support, compliant to CiA's 603 specification

Flexible Message Buffering and Filtering

- Configurable number of:
  - Receive buffers
  - Lower-priority transmit buffers
  - independently programmable 29-bit acceptance filters, 1 to 16
- One high-priority transmit buffer
- FIFO or priority mode for transmit buffers

Easy to Use and Integrate

- Programmable data rate up to 1 Mbit/s with CAN 2.0 and several Mbit/s with CAN FD or CAN XL option
- Programmable baud rate prescaler: 1 up to 1/256
- Single Shot Transmission Mode for lower software overhead and fast reloading of transmit buffer
- Programmable interrupt sources
- Generic 32-bit or 8-bit host-controller interface and optional 32-bit AMBA-APB, 32-bit AHB-Lite, 32-bit Wishbone, 32-bit Avalon-MM

Safety -Enhanced Version (optional)

- ISO-26262 ASIL-D Ready
- Implements ECC for SRAM and spatial redundancy for inner logic protection

Zero Risk

- Compatible with any CAN2.0 or CAN-FD transceiver (PHY)
- Multiple times production proven

Sourced from Fraunhofer IPMS

Functional Description

The CAN bus core is founded on the basic CAN protocol principle and meets all constraints of the CAN 2.0B and CAN FD specifications.

Several message buffers are used for buffering received or transmitted messages. The number of buffers can be selected before synthesis. Selecting a large number of buffers disables the need for real-time reaction to CAN messages for the host processor, which significantly eases software development of the system application.

The included high-priority primary transmit buffer (PTB) can be used to transmit an important message as fast as possible, even if several lower-priority messages are pending. The secondary transmit buffer (STB) operates either in FIFO mode or in priority mode where the order is changed depending on the message priority.

The host interface contains all the registers necessary to control and configure the core. The host is able to read and write these registers as conventional RAM in memory mapped mode.

The interface to the host is software configurable. All events on the CAN data bus or in the CAN controller core are signaled using an interrupt. Every interrupt source may be individually enabled or disabled. The CAN controller core contains up to sixteen software-programmable 29-bit acceptance filters that can be used to block unwanted CAN messages, reducing the load on the host controller.

The host controller interface operates in a different clock domain, which can be synchronous or asynchronous to the core clock. The host-interface type is 32-bit and can be customized with available wrappers to either an 8-bit-wide generic processor interface or a 32-bit-wide APB, AHB-lite interface, Wishbone, or Avalon-MM. This enables easy interfacing to many host controller types, facilitating quick integration with a microcontroller.

CAN XL Option

CAN XL is a new standard that is being developed by CAN in Automation (CiA). It supports larger payloads and offers data rates up to 10Mbit/s, providing a step between the classical CAN bus and faster protocols like Ethernet. CAN XL has all the advantages of the CAN protocol, and is interoperable with CAN 2.0 and CAN FD.

The CAN-CTRL core optionally supports CAN XL as defined by the latest version of CiA's 610-1 specification. The core will be modified, if needed, to remain compatible with future versions of CiA's specification and with future updates of the related ISO 11898-1 standard. Customer's purchasing the CAN-XL option will receive such updates as long as they remain under support and maintenance coverage.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Implementation Results

CAN-CTRL can be mapped to any ASIC technology or FPGA device (provided sufficient silicon resources are available). The following are sample results for the core configured with three receive buffers, three transmit buffers, and three acceptance filters (does not include priority mode, TTCAN and CiA603 timestamping,).

Configuration	Technology	Cell Area (eq. Gates)	Memory Bits
CAN 2.0	TSMC 40nm G	10,800	1,088
CAN 2.0	TSMC 28nm HPC	8,600	1,088
CAN FD	TSMC 40nm G	14,000	4,224
CAN FD	TSMC 28nm HPC	10.441	4,224
CAN XL	TSMC 28nm HPC	13,250	133,000

The next table provides sample results for the core configured with sixteen receive buffers, sixteen transmit buffers, sixteen acceptance filters, TTCAN, and 64-bit CiA603 timestamps,

Configuration	Technology	Cell Area (eq. Gates)	Memory Bits
CAN 2.0	TSMC 28nm HPC	8,700	5,920
CAN 2.0 - Safe	TSMC 28nm HPC	14,626	7,215
CAN FD	TSMC 28nm HPC	16,214	21,152
CAN-FD - Safe	TSMC 28nm HPC	39,714	25,779

Please contact CAST to get characterization data for your target configuration and technology.

Verification

The core has been rigorously verified through extensive synthesis, place and route, simulation runs, Verification IP, and plugfests. It has been embedded in numerous shipping customer products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms. It ships with everything required for successful implementation, including:

- VHDL or Verilog RTL source code, or targeted FPGA netlist
- Testbenches for behavioral, and post-synthesis verification
- Simulation and Synthesis scripts
- Linux driver
- User Documentation, and RUVM register descriptions

The optional safety-enhanced package further includes the Safety Manual (SAM), a Failure Modes, Effects and Diagnostics Analysis (FMEDA) and the ASIL-D Ready certificate, issued by SGS-TÜV Saar GmbH.