The JPEG-LS-D core implements a highly efficient and low-power, lossless and near-lossless image decompression engine that is compliant to the JPEG-LS, ISO/IEC 14495-1 standard. The decoder core can decompress any JPEG-LS stream or JPEG-LS payload of image container formats, such as DICOM (Digital Imaging and Communications in Medicine). It accepts compressed streams of images with up to 16-bit per color samples and up to four color components, in all widely used color subsampling formats. Supporting oversize image dimension parameters, the core can decode images with resolutions exceeding 64k x 64k pixels.

The easy-to-use JPEG-LS-D core operates on a standalone basis, parsing marker segments and decompressing coded data with no assistance from a host processor. The decoder reports the image format (i.e., resolution, subsampling format, and color sample-depth) to the system, so that the decoded images are properly further processed and/or displayed. Application (APP) or comment (COM) marker segments—which are typically used to embed metadata in the compressed stream—are also passed to the system via a dedicated interface.

SoC integration is straightforward thanks to standardized AMBA® interfaces. The core accepts compressed data and outputs pixel data, frame format information, and APP or COM marker segments via AXI4-Stream interfaces, and it provides access to its control and status registers via a 32-bit APB interface. A wrapper that bridges the AXI-Stream interfaces to AXI4 can optionally be delivered with the core.

The core is designed with industry best practices, and its reliability has been proven through both rigorous verification and silicon validation. The deliverables include a complete verification environment and a bit-accurate software model.

**Versions**

The core is available in two versions, size-optimized and scalable-throughput. The size-optimized version, JPEG-LS-DS, provides a throughput of one sample per cycle and requires only one image line of buffering. A single JPEG-LS-DS core can decompress several hundreds of Msamples per second when mapped on an ASIC technology.

The scalable-throughput version, JPEG-LS-DF, can process multiple samples per cycle by internally aggregating a user-defined number of JPEG-LS-DS cores. The JPEG-LS-DF is suitable for compressing images or video with ultra-high resolutions and/or frame rates but assumes the use of restart markers in the encoded stream.

**Block Diagram**

![Block Diagram of JPEG-LS-D](image)
Silicon Resources Utilization

The JPEG-LS-D can be mapped to any Microsemi device, provided enough silicon resources are available. The size of a core depends on its configuration. The following tables provide sample performance and resource utilization data for different Microsemi device families for the JPEG-LS-DS and JPEG-LS-DF versions of the core. The sample results do not represent the higher speed or smaller area for the core.

<table>
<thead>
<tr>
<th>Family/Device</th>
<th>Logic Resources</th>
<th>Memory Resources</th>
<th>Freq. (MHz)</th>
<th>Throughput (Msamples/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Igloo2 M2GL150-STD</td>
<td>13,358 4LUT</td>
<td>12 RAM64x18, 4 RAM1K18</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>PolarFire MPF500T-STD</td>
<td>12,910 4LUT</td>
<td>13 uSRAM, 6 LSRAM</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>RTG4 RT4G150-STD</td>
<td>12,943 4LUT</td>
<td>12 RAM64x18, 4 RAM1K18</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>SmartFusion2 M2S150-STD</td>
<td>13,358 4LUT</td>
<td>12 RAM64x18, 4 RAM1K18</td>
<td>30</td>
<td>30</td>
</tr>
</tbody>
</table>

Table 1: Sample results for the JPEG-LS-DS version of the core configured to support a max image width of 2018 pixels, 8 bits per sample, and 1 color component.

<table>
<thead>
<tr>
<th>Family/Device</th>
<th>Logic Resources</th>
<th>Memory Resources</th>
<th>Freq. (MHz)</th>
<th>Throughput (Msamples/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Igloo2 M2GL150-STD</td>
<td>22,950 4LUT</td>
<td>25 RAM64x18, 8 RAM1K18</td>
<td>30</td>
<td>60</td>
</tr>
<tr>
<td>PolarFire MPF500T-STD</td>
<td>22,715 4LUT</td>
<td>29 uSRAM, 8 LSRAM</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>RTG4 RT4G150-STD</td>
<td>22,794 4LUT</td>
<td>25 RAM64x18, 8 RAM1K18</td>
<td>25</td>
<td>50</td>
</tr>
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<td>25 RAM64x18, 8 RAM1K18</td>
<td>30</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 2: Sample results for the JPEG-LS-DF version of the core configured to support a max image width of 2018 pixels, 8 bits per sample, 1 color component, and 2 samples/cycle throughput.

Applications

The JPEG-LS-D is suitable for applications requiring numerically or visually lossless compression of images or video of potentially high color or greyscale accuracy such as medical imaging (DICOM), aerospace imaging/surveillance, and advanced driver assistance systems (ADAS).

JPEG-LS Compression Efficiency

Despite its lower computational complexity, JPEG-LS offers exceptionally high lossless compression efficiency. JPEG-LS is expected to outperform PNG, and to provide similar compression ratios as lossless JPEG2000 for both color and greyscale images. The following illustration shows several indicative examples.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in source code RTL (Verilog) or as an FPGA netlist, and its deliverables include everything required for successful implementation:

- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation and synthesis scripts
- Comprehensive user documentation

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