

Fraunhofer IPMS and CAST Announce a RISC-V Embedded Processor for Edge AI

RISC-V Summit, San Francisco, California — December 6, 2021 — Electronic systems research and development organization Fraunhofer IPMS and semiconductor intellectual property provider CAST, Inc. today announced an upcoming new option for the EMSA5-FS RISC-V processor that can perform artificial intelligence (AI) and machine learning (ML) functions in standalone devices.

Called “Edge AI,” this emerging capability enables devices to use AI and ML without relying on a connection to the cloud or other external processing systems. Moving this computing power to the standalone device provides dramatic decreases in latency and response

time—as an Edge AI device can make autonomous decisions within milliseconds—and overcomes poor Internet connections while also enhancing security. Edge AI is especially suitable for sensor data analysis, gesture control, vibration analysis, and more in automotive, consumer, industrial, and other applications.

Edge AI requires a capable but ultra-low-power and relatively inexpensive System on Chip (SoC). The [EMSA5-FS Processor](#) is well-suited to this use, and started shipping earlier this year. It is a 32-bit, single-issue, in-order, five-stage pipeline processor that supports the RISC-V open-standard instruction set architecture. It can include error correction and fault-tolerant features and is ready for ISO 26262 Functional Safety certification.

To add efficient AI functionality, Fraunhofer IPMS has focused on two new capabilities for the EMSA5-FS Processor:



- [TensorFlow Lite](#) is an open-source set of tools that enable on-device machine learning. It allows designers to run AI models on embedded, mobile, and Internet of Things (IoT) devices by addressing latency, privacy, size, and power consumption issues. Fraunhofer IPMS has ported TensorFlow Lite to the EMSA5-FS.
- [Zve Extensions to RISC-V](#) provide vector math processing for microcontrollers and embedded devices. They enable the fast execution of demanding functions — like AI and ML — in small, low-powered, edge devices. Fraunhofer IPMS is extending the EMSA5-FS core with the Zve instructions,

“These additions to the EMSA5-FS Processor core now enable the execution of vector instructions that allow parallel processing of datasets and can consequently improve performance as well as energy efficiency,” said Dr. Andreas Weder, group manager Module Integration at Fraunhofer IPMS. “Our users can now reliably implement Edge AI applications such as gesture recognition or vibration analysis.”

Designers developing systems with the EMSA5-FS Processor can exploit any open-source and commercial RISC-V aids, test tools, and libraries, including the GNU toolchain, the comprehensive Eclipse IDE with OpenOCD debug support, and the commercial Embedded Workbench® for RISC-V from IAR Systems.

The new TensorFlow Lite AI option for the EMSA5-FS should be available through CAST in the first half of 2022, with the Zve Extensions to follow. Inquiries are welcome now at info@cast-inc.com or +1 202.392.8300, and those interested are invited to stop by CAST’s sponsor area at the [RISC-V Summit](#) Dec. 6–8, 2021 (Kiosk K6).

Learn more about Fraunhofer IPMS at www.ipms.fraunhofer.de, and about CAST, Inc. at www.cast-inc.com.

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