EMAC-1G
Gigabit Ethernet Media Access Controller

XILINX

Implements an Ethernet Media Access Controller compatible with the 10/100 Mbps IEEE 802.3 and 1Gbps IEEE 802.3-2002 specifications. The controller provides half- or full-duplex operation, supports jumbo frames, and optionally provides a useful set of statistics counters enabling station management. Furthermore, the core can optionally be configured with a hardware timestamping unit enabling support for the IEEE 1588 precision time protocol (PTP).

A host processor can control the operation of the core via a slave interface that provides access to its control and status registers. The EMAC-1G features two master ports for data transfers, one for transmit and one for receive. The two DMA engines use buffer descriptors to automatically transfer data from local FIFOs to an external shared memory. The core supports 32-bit AMBA/AHB or Wishbone SoC buses; other bus interfaces are available on request.

Integration with an Ethernet PHY is straightforward, as the controller core supports the Media Independent Interface (MII) and the Gigabit Media Independent Interface (GMII) physical layer interface standards.

The EMAC-1G is production proven in ASIC and FPGA technologies.

Applications

The EMAC-1G can be used in any SoC design requiring Ethernet connectivity. Half-duplex operation and high-accuracy timing synchronization makes it ideal for automotive, and industrial networks using a single twisted pair like 10BASE-T1S, 10BASE-T1L and 100BASE-T1. The core is equally efficient in systems using conventional full-duplex connections.

Block Diagram
**Implementation Results**

The EMAC-1G can be mapped to any ASIC technology or FPGA device (provided sufficient silicon resources are available). The following table provides sample Xilinx performance and resource utilization data. The provided figures do not represent the higher speed or smaller area for the core. Please contact CAST to get characterization data for your target configuration and technology.

<table>
<thead>
<tr>
<th>Family</th>
<th>Slices</th>
<th>Fmax (MHz)</th>
<th>RAM Blocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Artix-7 xc7a200tbg676-1</td>
<td>1120</td>
<td>125</td>
<td>4 RAMB18</td>
</tr>
<tr>
<td>Kintex-7 xc7k160tbg676-1</td>
<td>1068</td>
<td>156</td>
<td>4 RAMB18</td>
</tr>
<tr>
<td>Virtex-7 xc7vx330tffg1157-1</td>
<td>1098</td>
<td>146</td>
<td>4 RAMB18</td>
</tr>
</tbody>
</table>

**Verification**

The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

**Support**

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

**Deliverables**

The core is available in Verilog RTL or as targeted FPGA netlist, and its deliverables include everything required for a successful implementation, including an extensive testbench, comprehensive documentation and a sample Linux driver.