JPEG-E-T

Tiny Baseline JPEG Encoder

XILINX

This JPEG compression IP core supports the Baseline Sequential DCT and the Extended Sequential DCT modes of the ISO/IEC 10918-1 standard. It implements an area-efficient, hardware JPEG encoder with very low processing latency. Probably the smallest JPEG encoder IP core in the marker, the JPEG-EX-T occupies about 3,000 LUTs when implemented in a Xilinx FPGA.

The encoder processes one color sample per clock cycle, enabling it to compress multiple Full-HD channels even in low-cost FPGAs. Once programmed, the easy-to-use encoder requires no assistance from a host processor to compress an arbitrary number of frames.

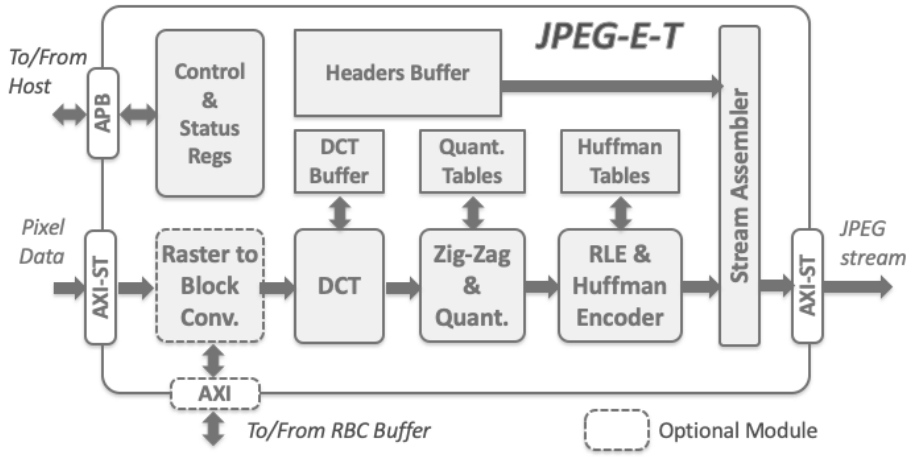
SoC integration is straightforward thanks to standardized AMBA® interfaces: AXI Streaming for pixel and compressed data, and a 32-bit APB slave interface for registers access. Users can optionally insert timestamps or other metadata in the compressed stream using a dedicated AXI Streaming interface.

The core is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-E-T core is suitable for systems supporting ultra-high frame resolutions and/or frame rates, such as: Corporate, airborne, and other security or surveillance systems, machine vision and video link decoders or terminals for industrial, or defense systems and medical imaging systems

Block Diagram



Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive synthesis, place and route, and simulation runs. It has been embedded in several shipping customer products, and is proven in both ASIC and FPGA technologies.

Deliverables

The core is available as a targeted FPGA netlist and includes everything required for successful implementation. The deliverable package includes:

- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation scripts
- Comprehensive user documentation

FEATURES

Extremely small JPEG encoder

Standards Support

- ISO/IEC 10918-1 Standard Baseline Encoder (Sequential DCT modes)
- Encodes single-frame JPEG images and Motion JPEG payloads
- 8-bit o 12-but per color sample
- Up to four color components; any image size up to 64k x 64k
- Handles all scan configurations and all JPEG formats
- APP, COM, and restart markers
- Programmable Quantization table, for image quality or bit-rate control

Interfaces

- AXI Streaming input and output data interfaces
- APB Control/Status interface
- Optional AHB wrapper with DMA capabilities

Performance and Size

- One encoded sample per clock cycle
- Small silicon footprint (~3,000 LUTs)

Ease of Integration

- Automatic program-once/encode-many operation
- Simple, dedicated timestamps interface
- Included bit-accurate software model generates test vectors, expected results, and core programming values
- Optional Raster-to-Block Conversion with AXI or standard memory interface to the lines buffer

Format

- Available as a targeted FPGA netlist

Sourced from BEYOND SEMICONDUCTOR

JPEG Cores Available from CAST

This core is one member of the family of JPEG encoder and decoder cores that CAST offers. The following table summarizes the family members and indicates their basic features.

JPEG IP Cores	**JPEG-E-T** Tiny Baseline JPEG Encoder	**JPEG-E-S** Baseline JPEG Encoder	**JPEG-EX-S** Extended JPEG Encoder	**JPEG-EX-F** Ultra Fast Ext. JPEG Encoder	**JPEG-D-S** Baseline JPEG Decoder	**JPEG-DX-S** Extended JPEG Decoder	**JPEG-DX-F** Ultra Fast Ext. JPEG Decoder
Functionality	Encoder				Decoder		
Baseline JPEG	✓	✓	✓	✓	✓	✓	✓
Extended Sequential JPEG	×	×	✓	✓	×	✓	✓
Motion JPEG Payload	✓	✓	✓	✓	✓	✓	✓
Sub-sampling Formats	Any with up to four components including Single–color, 4:4:4, 4:2:2, 4:2:0						
Image Resolution	16x16 to 64k x 64k						
Max. Sample Depth	8	8	12	12	8	12	12
Programmable Huffman Tables	×	✓	✓	✓	N/A	N/A	N/A
Rate Control	×	✓	✓	✓	N/A	N/A	N/A
Raster Conversion	Included – Optionally Instantiated						
Color Samples/Cycle	1	1	1	1 to 32	1	1	1 to 32
Number of LUTs in Xilinx FPGAs	3k	5k	6k	11k[1]	5k	6k	10k[1]
Available in RTL Source Code	×	×	✓	✓	×	✓	✓
Available as targeted netlist	✓	✓	✓	✓	✓	✓	✓

1) Silicon Resources for two samples/cycle configuration, and 12 bits per color sample