JPEG-D-S

Baseline JPEG Decoder

This JPEG decompression IP core supports the Baseline Sequential DCT mode of the ISO/IEC 10918-1 standard. It implements a high-performance hardware JPEG decoder that is very small in silicon area.

The JPEG-D-S Decoder decompresses JPEG images and the video payload for Motion-JPEG container formats. It accepts compressed streams of images with 8-bit color samples and up to four color components, in all widely-used color subsampling formats.

The decoder processes one color sample per clock cycle, enabling it to process multiple Full-HD channels even in low-cost FPGAs. One of the smallest JPEG decoders available, it requires approximately 6,500 LUTs when mapped on a Xilinx FPGA.

Once programmed, the easy-to-use decoder operates on a standalone basis, parsing marker segments and decompressing coded data with no assistance from a host processor. The decoder reports the image format (i.e., resolution, subsampling format, and color sample-depth) to the system, so that the decoded images are properly further processed and/or displayed.

SoC integration is straightforward thanks to standardized AMBA® interfaces: AXI Streaming for pixel and decompressed data, and a 32-bit APB slave interface for registers access.

Customers with a short time to market requirements can use CAST's IP Integration Services to receive complete JPEG subsystems. These integrate the JPEG decoder with video interface controllers, Hardware UDPIP or Transport Stream networking stacks, or other IP cores available from CAST.

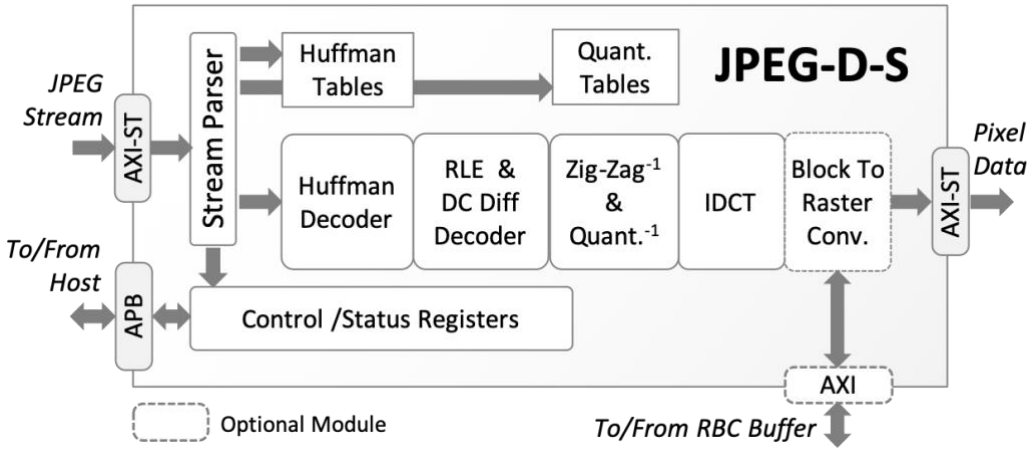
The core is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. Its deliverables include a complete verification environment and a bit-accurate software model.

Applications

The JPEG-D-S core's excellent performance and low silicon resource usage make it suitable for implementing a variety of digital imaging applications, including:

- Residential, corporate, airborne, and other security or surveillance systems.
- Machine vision and video link decoders/terminals for industrial, defense, or other systems.
- Medical imaging system, and advanced driver assistance systems.

Block Diagram



FEATURES

Area-efficient, high-performance Baseline JPEG decoder for Xilinx FPGA

Standards Support

- ISO/IEC 10918-1 Standard Baseline Decoder
- Single-frame JPEG images and Motion JPEG payloads
- Up to four color components
- 8-bit color samples
- All widely used color subsampling formats, and any image size up to 64k x 64k
- All scan configurations and all JPEG formats
- All marker segments expect DNL
- Up to four Huffman Tables
- Up to four 8-bit or 16-bit Quantization tables

Interfaces

- AXI Streaming I/O data interfaces
- APB Control/Status interface
- Optional AHB wrapper with DMA capabilities

Performance and Size

- One decoded sample per clock cycle
- Small silicon footprint (~6.5k LUTs)

Ease of Integration

- Requires no programming or control from host
- Reports image format
- Detects and reports marker syntax errors
- Delivered with bit-accurate software model
- Optional Block-to-Raster Conversion with AXI or standard memory interface towards the lines buffer

Format

- Available as a targeted FPGA netlist

Silicon Resources Utilization

The JPEG-D-S can be mapped to any Xilinx Device (provided sufficient silicon resources are available) and optimized to suit specific project requirements. The following table provides sample implementation and performance data for the default configuration of the core.

Family	1080p30 4:2:2	1080p30 4:2:0	LUTs	DSPs	BRAMs
Artix7 (-2)	✔	✘	6,500	5	2
Kintex7 (-2)	✔	✔			
Kintex7-US (-1)	✔	✔			

Note that the list of video formats is not exhaustive, and that these sample implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to get characterization data for your target configuration and technology.

Verification

The core has been verified through extensive synthesis, place and route and simulation runs. It has also been embedded in several products and is proven in both ASIC and FPGA technologies.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available as a targeted FPGA netlist and includes everything required for successful implementation. The XIlinx version includes:

- Netlist
- Sophisticated self-checking Testbench
- Software (C++) Bit-Accurate Model
- Sample simulation scripts
- Comprehensive user documentation

JPEG Cores Available from CAST

This core is one member of the family of JPEG encoder and decoder cores that CAST offers. The following table summarizes the family members and indicates their basic features.

JPEG IP Cores	JPEG-E-T Tiny Baseline JPEG Encoder	JPEG-E-S Baseline JPEG Encoder	JPEG-EX-S Extended JPEG Encoder	JPEG-EX-F Ultra Fast Ext. JPEG Encoder	JPEG-D-S Baseline JPEG Decoder	JPEG-DX-S Extended JPEG Decoder	JPEG-DX-F Ultra Fast Ext. JPEG Encoder
Functionality	Encoder				Decoder		
Baseline JPEG	✔	✔	✔	✔	✔	✔	✔
Extended Sequential JPEG	✘	✘	✔	✔	✘	✔	✔
Motion JPEG Payload	✔	✔	✔	✔	✔	✔	✔
Sub-sampling Formats	Any with up to four components including Single–color, 4:4:4, 4:2:2, 4:2:0						
Image Resolution	16x16 to 64k x 64k						
Max. Sample Depth	8	8	12	12	8	12	12
Programmable Huffman Tables	✘	✔	✔	✔	N/A	N/A	N/A
Rate Control	✘	✔	✔	✔	N/A	N/A	N/A
Raster Conversion	Included – Optionally Instantiated						
Color Samples/Cycle	1	1	1	1 to 32	1	1	1 to 32
Number of LUTs in Xilinx FPGAs	3k	5k	6k	11k[1]	5k	6k	10k[1]
Available in RTL Source Code	✘	✘	✔	✔	✘	✔	✔
Available as targeted netlist	✔	✔	✔	✔	✔	✔	✔

1) Silicon Resources for two samples/cycle configuration, and 12 bits per color sample