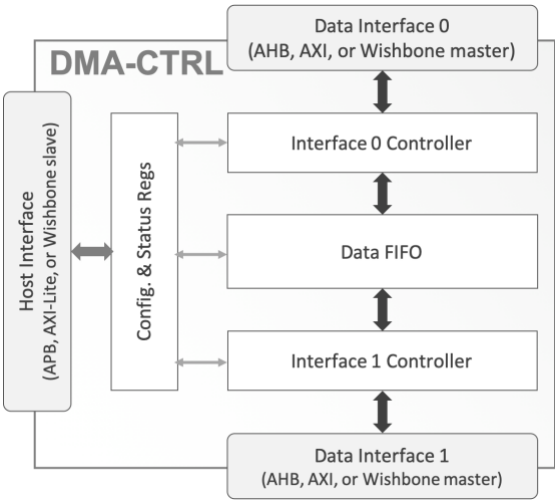
# DMA-CTRL

## AHB/AXI/Wishbone DMA Controller

The DMA-CTRL core implements a low-power, highly configurable Direct Memory Access (DMA) controller that transfers data over AHB, AXI, or Wishbone busses.

With the DMA-CTRL, a DMA transfer can be initiated by software (via register access), or via a dedicated DMA-request pin that can be driven by a peripheral or other hardware modules. The latter makes the core suitable for low-power systems where, in order to preserve power, it may be desirable to transfer data upon a schedule or when an event occurs, without waking up the CPU.

The core's configuration and status registers are accessible via a 32-bit host slave interface. The protocol for the host slave interface is configurable at synthesis time, and the user can choose between a Wishbone, AMBA® AXI Lite, or AMBA® APB interface. The core's registers are used to configure the DMA transfer parameters, such as the number of bytes to be transferred, transfer direction, address offsets, bus addressing mode, and burst size. The core also reports possible transfer status and possible bus errors to its status registers.




The core has two master interfaces for transferring data: the one reads data from the source location and the other writes data to the destination location. The protocol for each master port is configurable at synthesis time, and the user can choose between a Wishbone, AXI, or AHB interface. The direction of the transfer is run-time programmable, and the user can choose to implement a different protocol for each interface. This means that the DMA-CTRL core can be used to transfer data between different buses (e.g. AHB and AXI, or AXI to Wishbone). If the same protocol is used for both master ports, then the two ports can be externally arbitrated and be connected to a single master port of the interconnect fabric.

The DMA-CTRL core is rigorously verified, silicon-proven, and available in RTL Verilog source or as a targeted FPGA netlist.

### FEATURES

- Low-power DMA controller, supporting software- and hardware-triggered DMA transfers.
- Highly configurable: can transfer data between AMBA® AHB, AMBA® AXI, and Wishbone buses

#### Programmable Options

- Transfer size
- Source and destination base address
- Address-increment mode
- Bus burst length
- Enable/disable hardware triggered mode

#### Configuration Options

- Register interface
  - AMBA AXI Lite Slave
  - AMBA APB Slave
  - Wishbone Slave
- Data interface
  - AMBA AXI Master
  - AMBA AHB Master
  - Wishbone Master
- Data and address width for the data interfaces
- Internal FIFO size

#### Deliverables

- Synthesizable Verilog RTL or FPGA netlist
- Testbench & sample test cases
- Simulation & synthesis scripts
- Documentation

## Applications

The DMA-CTRL core can be used in numerous systems where massive data transfers occur. These applications may include networking systems, disk controllers, encryption and decryption systems, display modules and graphic accelerators, data processing and other intense data requiring architectures. Multiprocessor systems are another example where DMA transfers may be desired.

## Support

The DMA-CTRL as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are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