S80251XC3

Super-Fast, Configurable 16-bit 80251 Microcontroller

The S80251XC3 core implements a high-performance 16-bit microcontroller that executes the MCS®251 & MCS®51 instruction sets and includes a configurable range of features and integrated peripherals.

The core's advanced architecture yields the fastest 8051/80251-compatible MCU available anywhere (at the time of its release). It employs separate instruction and data buses (Harvard architecture), branch prediction, branch target caches, and stacking/un-stacking speed up features, and is able to execute some instructions in parallel. Dhrystone 2.1 tests show it to run 69.7 times faster than the original 8051 at the same frequency, without requiring an external arithmetic acceleration unit (such as an MDU). Representative 40nm ASIC implementations can run with clock frequencies in excess of 240MHz, offering an effective speed up of more than 1,400 times over early 8051 chips.

The S80251XC3 is also extremely energy efficient. Its small silicon footprint—the complete microcontroller (CPU and peripherals) can be under 35,000 gates in size—means there is very little power leakage. Its higher performance compared to other 8-bit or 16-bit MCUs allows clocking at lower frequencies. Users can also adjust the core's energy consumption to match the processing workload via dynamic frequency scaling and independent control of the CPU and peripherals clocks.

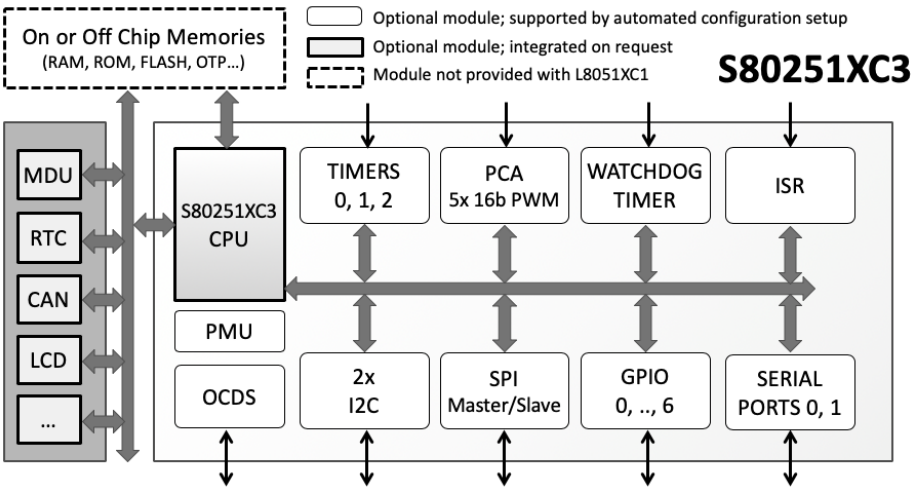
The core has a rich set of optional features and pre-integrated peripherals, allowing function, performance, and area to be balanced for each specific application. Software development is facilitated by a single-wire or JTAG debugging interface that operates seamlessly within the ARM® Keil® C251 integrated development environment. Inexpensive debug pods and a complete reference design board package are available.

This 80251 core builds on CAST's experience with hundreds of 8051 IP customers going back to 1997. Designed for easy reuse in ASICs or FPGAs, the core is strictly synchronous, with positive-edge clocking (except in the optional debug & SPI modules), synchronous or asynchronous reset, and no internal tri-states.

Applications

The S80251XC3 is a low-power and cost-effective processor that can be used for a variety of tasks, either as a peripheral microcontroller in complex SoCs, or as the main embedded processor in mixed signal ICs.

Block Diagram



FEATURES

Fully compatible with the MCS®251 & MCS®51 instruction sets

Ultra-High Performance

- 0.655 DMIPs/MHz for a 69.7x speed up over the original 8051 at the same clock frequency
- More than 1,400 times faster than the original 8051 when clocked at maximum frequency

Energy Efficient

- Small silicon footprint for lower leakage and less static power
- Higher DMIPs/MHz allows saving power by operating at lower clock frequency
- Advanced power management supports dynamic frequency scaling and CPU and/or peripherals clock gating

Configurable Microcontroller

- Automatic instantiation of user selectable MCU peripherals
- Pre-integration with other CAST IP on request
- Configurable CPU and memory architecture to match application needs

Easy Firmware Development

- CDP-XC on-chip debug interface, supports JTAG and Single-Wire
- USB-to-Serial and USB-JTAG, low cost CDP-XC debug pods
- Seamless integration with Keil uVision™
- Software and Hardware breakpoints

Flexible Memory Architecture

- 16MB program and data address space; 64kB stack space
- Acknowledged transactions feature makes integration with slow memoires or peripherals easy
- 6x32-bit additional general purpose registers
- Independent program and data buses

Efficient and Rapid Interrupts Handling

- Up to 23 interrupts, with two or four interrupt priority levels
- Ultra-low interrupt latency: two cycles from interrupt assertion to ISR routine start

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Peripherals and Options

The S80251XC3 allows the user to easily select among a rich set of pre-integrated and pre-verified peripherals and core configuration options. Simple Verilog defines (e.g. “define USE_PMU”) are used for that purpose. The following list summarizes the peripherals and configuration options that are available. Those noted with an asterisk are not included by default with the S80251XC3, but can be added on request.

Timers/Counters

- **Timer 0 & 1**: 80C51-like 16-bit timers/counters
- **Timer 2**: 8052-like 16-bit counter
- **PCA**: 80251-like programmable counter array with five PWM channels
- **WDT**: 80251-like Watchdog Timer

Interfaces

- **I2C 0 & 1**: Master-Slave ports for Phillips Inter-Integrated Circuit (I2C) serial bus
- **SPI**: Master-Slave port for Serial Peripheral bus Interface serial bus
- **Serial 0**: 80C51 or 80251-like Full-Duplex UART/USART
- **GPIO 0-4**: 80C51-like 8-bit Input / Output parallel ports
- **SFR**: Special Function Registers interface
- **ISR**: 80251-like Interrupt Controller with up 23 sources, and two or four priority levels
- **GPIO 5***: 80C515-like parallel port 5
- **CAN***: Controller Area Network Bus 2.0 and Flexible Data (FD) Controller
- **LIN*:** Local Interconnect Network Bus Controller
- **OCDS**: On-chip debugging system interface

Performance Acceleration & Architectural Options

- **AIEA**: Advanced instruction execution architecture, which includes a number of performance optimizations
- **VDMA***: Direct Memory Access controller, with up to 8 channels
- **32MIF:** 32-bit memory code/date memory interface
- **PMU:** Power management unit

Sample Implementation Results

The following are sample ASIC pre-layout results and do not represent the absolute highest speed or smallest area possible. (Area figures do not include memories.)

Configuration	Technology	Clock Frequency	Area
S80251XC3–CPU (CPU-only)	40nm	240 MHz	27,366 eq. Gates
S80251XC3 (CPU, peripherals*, no-OCDS)	40nm	188 MHz	49,174 eq. Gates

- 3xTimer, PCA, UART, WDT, GPIO

Deliverables

The core is available in Verilog RTL or as a targeted FPGA netlist. Its deliverables include everything required for a successful implementation, including a behavioral model, an automated constrained random verification (CRV) testbench, comprehensive documentation, and sample synthesis and simulation scripts.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available; contact CAST Sales.