PCI-T32

32-bit/33MHz PCI Target Core

The PCI-T32 implements a target PCI interface compliant with the PCI 2.3 specification. It supports a 32-bit address/data bus and operates up to 33 MHz PCI clock.

The interface core implements 64 bytes of PCI Configuration Space registers. It is possible to extend the Configuration Space up to 256 bytes if required.

The Target supports up to six Base Address Registers with both I/O and Memory space decoding from 16 bytes up to 4 GB.

The Target supported commands are:

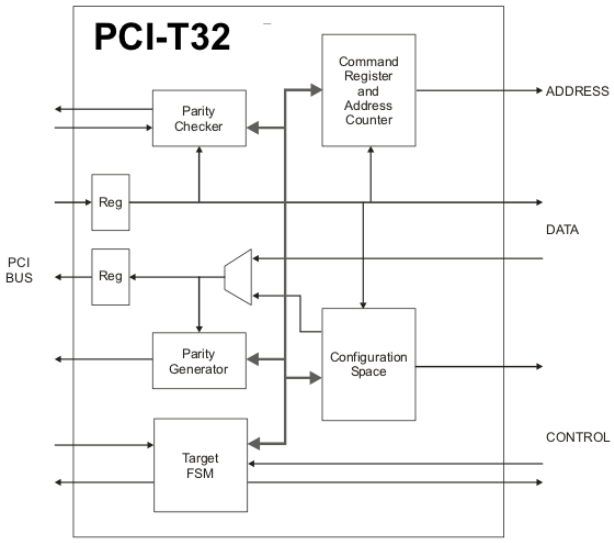
- Configuration Read, Configuration Write
- Memory Read, Memory Write, Memory Read Multiple (MRM), Memory Read Line (MRL), Memory Write and Invalidate (MWI)
- I/O Read, I/O Write

FEATURES

- PCI specification 2.3 compliant
- 33 MHz performance32-bit datapath
- Zero wait states burst mode
- Full Target functionality
- Single interrupt support
- Type 0 Configuration space
- Support of all Base Address Registers
- Support of backend initiated target retry, disconnect and abort
- Parity generation and parity error detection
- Optional bridge / interface to AMBA/AHB or Avalon-MM
- Available in synthesizable HDL source code
- Silicon-proven

The PCI-T32 builds on more than 15 years of CAST PCI IP expertise and has been designed for straightforward reuse, with proven design practices that ensure easy integration and smooth technology mapping. The core is available in synthesizable RTL or as a targeted FPGA netlist, and is delivered with everything required for rapid and successful integration and implementation.

Block Diagram



Core Configuration

The customer can adjust the PCI-T32 core parameters in the RTL. For a netlist license the delivered netlist is generated with the parameters specified by the customer.

The PCI-T32 core can support 66 MHz PCI bus speed. Depending on the target technology a minor modification might be required. Please contact CAST for any required information.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The core has been verified through extensive simulation and rigorous code coverage measurements.

Deliverables

The core is available in ASIC (synthesizable HDL) and FPGA (netlist) forms, and includes everything required for successful implementation. The ASIC version includes:

- HDL RTL source code
- Sophisticated HDL Testbench
- Simulation script, vectors, expected results, and comparison utility
- Synthesis script
- Comprehensive user documentation, including detailed specifications and a system integration guide

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