# GPIO-APB

## General-Purpose I/O Controller with APB Interface

The GPIO-APB core is used to create functions in a system that are not implemented with dedicated controllers, and require simple input and/or output software-controlled signals.

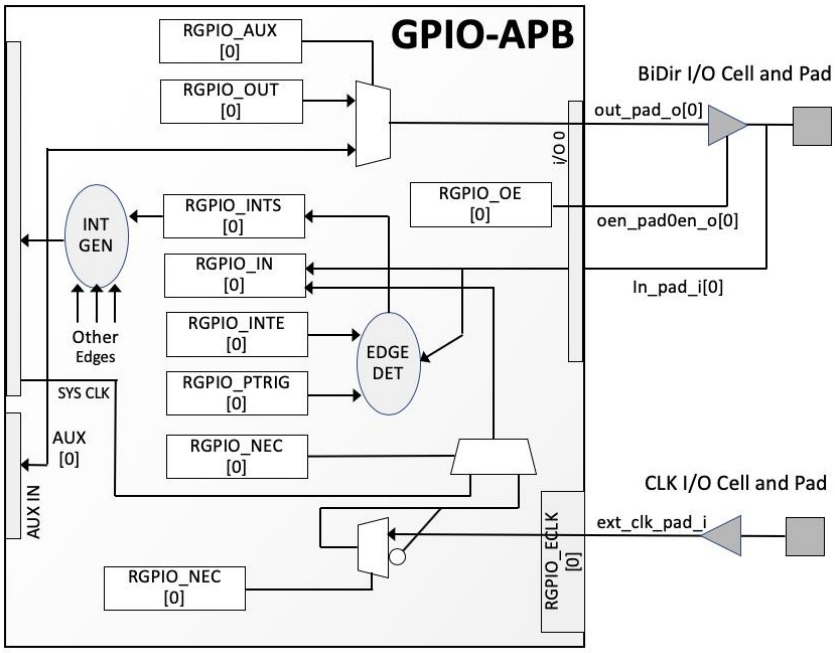
The number of general-purpose I/O signals is user selectable ranging from 1 to 32. For more I/O signals, several GPIO cores can be used in parallel. Each GPIO-APB signal can be programmed individually as an input, an input in interrupt mode, an output, a bi-directional I/O, or as driven by an auxiliary input. GPIO signals programmed as inputs can be registered at the rising edge of the system clock or at a user-programmed edge of the external clock.

The GPIO-APB core is rigorously verified, silicon-proven and available in RTL source or as a targeted FPGA netlist.

## Applications

The GPIO-APB core can be used in a wide range of applications where simple I/O control is needed.

## Block Diagram




## FEATURES

- User selectable number of GPIO signals from 1 to 32
- All GPIO signals can be bi-directional (external bi-directional I/O cells are required in that case)
- All GPIO signals can be tri-stated or open-drain enabled (external tri-state or open-drain I/O cells are required in that case)
- GPIO signals programmed as inputs can cause an interrupt request to the CPU
- All GPIO signals are programmed as inputs at hardware reset
- Auxiliary inputs to the GPIO core bypass outputs from RGPIO_OUT register
- Alternative input reference clock signal from external interface
- 32-bit APB interface (contact CAST for other interfaces)
- Extremely configurable (implementation of registers, external clock inverted versus negative edge flip-flops etc.)

### Deliverables

- Synthesizable RTL or FPGA netlist
- Testbench & sample test cases
- Simulation & synthesis scripts
- Documentation

## Support

The GPIO-APB as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.