

# AXI2APB

## AXI to APB Bus Bridge

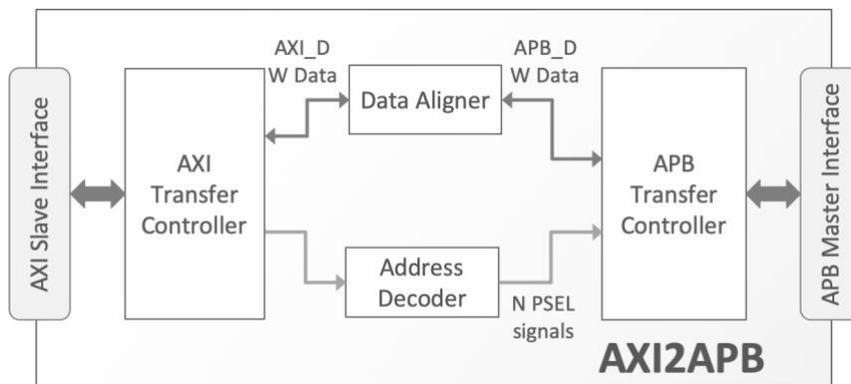
The AXI2APB implements a bridge between AXI and APB buses, allowing the connection of peripherals with an APB interface to an AXI bus.

The highly configurable core translates read or write transactions on the AXI bus to APB bus transactions. An AXI4 master, such a microprocessor, can connect to its AXI slave interface, and APB4, APB3, or APB2 peripherals can connect to its APB master port. Furthermore, the endianness and the data bus widths of the AXI and APB interfaces are independently configurable.

The user can also select the number of APB slaves and their address mapping at synthesis time. To ease core configuration, the core's deliverables include a software application, that enables users to configure the core via an intuitive HTML interface and automatically generate the corresponding Verilog parameter values.

The LINT-clean and scan-ready AXI2APB core is extensively verified and proven in multiple production designs. It can be mapped to any ASIC or FPGA, provided sufficient silicon resources are available, and it is delivered with everything required for successful implementation including a testbench and comprehensive documentation.

### Block Diagram



### Support

The AXI2APB as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

### FEATURES

#### AMBA™ AXI to APB Bridge

- Allows connecting APB slaves to an AXI master
- Supports AXI4 host and APB4, APB3 or APB2 Slaves

#### Configuration Parameters

- AXI data bus width and endianness
- APB data bus width (can be different than AXI data bus width)
- APB address bus width
- Number of APB Slaves
- Data width, base address, and address space per APB Slave
- Use of write strobe (PSTRB) and error response (PSLVERR) signal per slave

#### Easy to Use and Integrate

- Requires no run-time programming or initialization
- HTML configuration tool generates Verilog parameters
- Fully synchronous, scan-ready, LINT-clean design
- Delivered with sample scripts, RTL testbench, and sample test cases