

AXI-SBS

AXI Subsystem

The AXI-SBS is an integrated, verified, AMBA® compliant hardware/software system ready for embedded applications using processors with AXI4 interfaces such as the BA20, BA21, and several RISC-V Implementations.

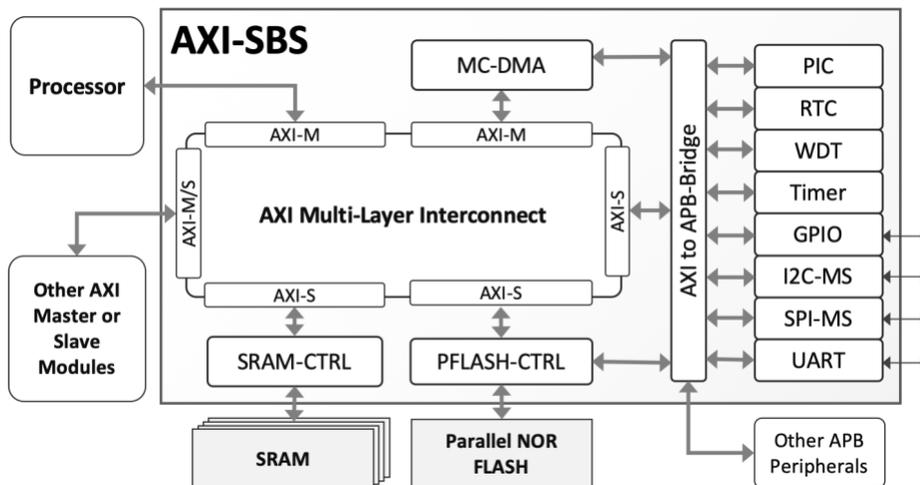
The AXI Subsystem combines peripheral and interface IP cores with drivers and other essential software and an AXI/APB bus infrastructure. It is designed to work well with the user's choice of processor, and has been specifically tested with those from CAST.

The AXI-SBS integrates a 32-bit multilayer AXI fabric with an SRAM controller, a multi-channel DMA controller, an external memory controller, suitable for accessing off-chip parallel NOR-flash devices or SRAMs, an APB bridge, and a set of APB peripherals, such as timers and serial interfaces.

The AXI-SBS was designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. It is delivered in human-readable Verilog source code along with comprehensive documentation for each module, example drivers, and software exercising all the peripherals.

This subsystem can be mapped to any Intel, Lattice, MicroSemi, or Xilinx programmable device, or to any ASIC technology, provided sufficient silicon resources are available. Please contact CAST Sales to get accurate characterization data for your specific implementation requirements.

Block Diagram



Integration and Customization Services

CAST engineers can provide integration and customization services to help you further reduce your time to market. Extremely experienced with both system hardware and custom software development, they are ready to work with you at any stage of the design process from architecture to implementation to system level verification to production readiness. Contact CAST Sales to learn more.

FEATURES

Subsystem for uP with 32-bit AMBA® AXI4 interfaces such as:

- BA20, BA21, BA22-DE, BA22-CE
- Several RISC-V processors

Integrated Modules

- AXI multi-layer fabric
- Multichannel DMA
- Internal SRAM Controller
- External parallel flash or SRAM controller
- AXI-to-APB Bridge
- APB Peripherals:
 - I2C Master/Slave
 - Octal SPI Master/Slave
 - 16550 UART
 - GPIO
 - Real-Time Clock
 - Generic Timer
 - Watchdog Timer
 - Programmable Interrupt Controller

Configuration Options

- Number of AXI master, AXI slave and APB slave ports for user's modules
- APB-slave port access per master
- Arbitration scheme per AXI slave-port

Customization Options

- Integration with CAST or 3rd party IPs