AXI-MLIC

AXI Multilayer Interconnect

The AXI-MLIC is a multilayer AMBA® AXI bus interconnect fabric connecting an arbitrary number of bus masters to an arbitrary number of slaves.

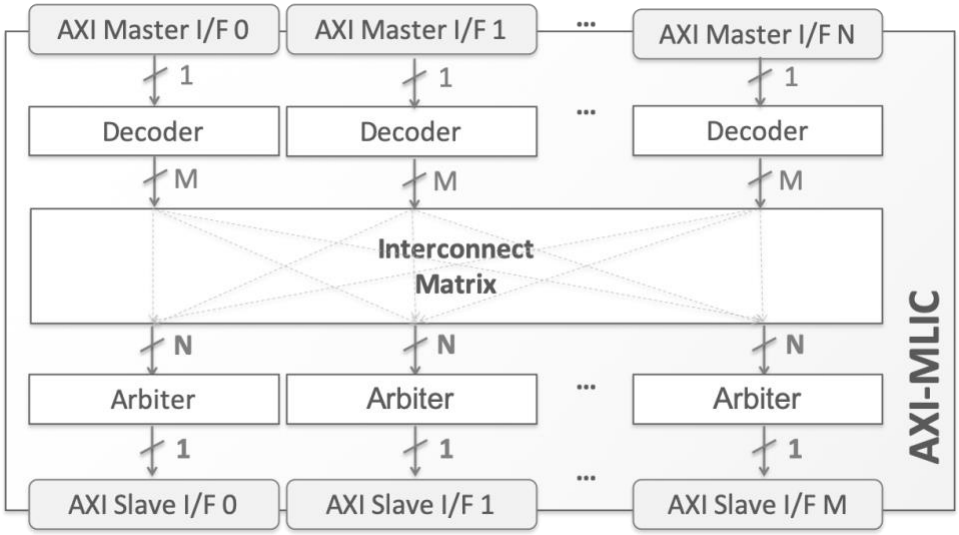
The AXI fabric offers high interconnect throughput, as arbitration is performed at the slave port and therefore masters do not compete for bus control. In practice, each master accesses the peripherals connected to the slave ports via a dedicated bus, and only competes with others when they attempt to access the same peripheral at the same time.

The highly configurable AHB-MLIC allows users not only to define the number of master ports and the number of slave ports, but also to define the slaves' base address and address space per master port. The bit widths for the address bus, data bus, and master and slave identification signals are also user selectable, as is the access arbitration scheme.

When two or more masters attempt to read or write the same peripheral, access is granted to one of them using a priority-based, or round-robin, or mixed (priority and round-robin) arbitration scheme. The user can choose different arbitration schemes for each slave port. To ease core configuration, the deliverables include a software application that enables users to configure the fabric via an intuitive HTML interface and automatically generate the corresponding Verilog parameter values.

The LINT-clean and scan-ready AXI-MLIC core is extensively verified and proven in multiple production designs. It can be mapped to any ASIC or FPGA, provided sufficient silicon resources are available, and it is delivered with everything required for successful implementation including a testbench and comprehensive documentation.

Block Diagram



FEATURES

Configurable AMBA® AXI4 Interconnect Fabric

- Arbitrary number of master ports
- Arbitrary number of slave ports
- User-defined bit width for:
  - AXI Data bus (9-1024)
  - AXI Address bus (1-64)
  - AXI Master and slave ID signals (1-64).
- User-defined slave to master mapping
  - Slaves access can be disabled to one or more masters.
- User-defined slave base address and address space per master
  - A slave address can be different between masters.
- Flexible arbitration: Priority-based, or round-robin, or mixed arbitration selectable per slave

High Throughput

- Less arbitration overhead between masters, as arbitration is done at each slave port

Easy to Use and Integrate

- Requires no run-time programming or initialization
- HTML configuration tool generates Verilog parameters
- Fully synchronous, scan-ready, LINT-clean design
- Delivered with sample scripts, RTL test-bench and sample test-cases

Support

The AXI-MLIC as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

www.cast-inc.com • info@cast-inc.com • tel +1 201.391.8300

Sourced from BEYOND SEMICONDUCTOR