The APB-SBS subsystem integrates typical microcontroller peripherals connected on the an AMBA® APB bus with a bridge to an AHB or AXI bus. The subsystem is ready for integration with processors having either an AHB or an AXI interface such as the BA2x processors, and several ARM Cortex and RISC-V processors.

The peripherals connect to the 32-bit APB ports of the APB bridge, which allows configuring the base address and the size of the address space for each peripheral. The subsystem includes the following peripherals:

- I2C Master & Slave
- Single/Dual/Quad/Octal SPI Master & Slave
- 16550-compatible UART
- 32 GPIOs
- Real-Time Clock
- Watchdog Timer
- Generic Timer
- Programmable Interrupt Controller

Other peripherals with a 32-bit APB interface can be connected to the subsystem, via a configurable number of extra 32-bit APB ports. Each of the extra APB ports are configured independently to comply to APB2, APB3 or APB4 standard. The APB-SBS was designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. It is delivered in human-readable Verilog source code along with comprehensive documentation for each module, example drivers, and software exercising all the peripherals.

This subsystem can be mapped to any Intel, Lattice, MicroSemi, or Xilinx programmable device, or to any ASIC technology, provided sufficient silicon resources are available. Please contact CAST Sales to get accurate characterization data for your specific implementation requirements.

Block Diagram

![Block Diagram](image)

**Integration and Customization Services**

CAST engineers can provide integration and verification services to help you further reduce your time to market. Extremely experienced with both system hardware and custom software development, they are ready to work with you at any stage of the design process from architecture to implementation to system level verification to production readiness. Contact CAST Sales to learn more.