SRAM-CTRL
Static RAM Controller

The SRAM-CTRL implements a Static Random Access Memory (SRAM) Controller translating AHB, or AXI4, or APB bus reads and writes into reads and writes with the signaling and timing of a standard 32-bit synchronous SRAM. The type of host interface is user-defined at synthesis time.

When the AHB interface is selected, the SRAM controller provides zero-wait-state AHB access to the synchronous SRAM in all cases except for the following back-to-back events: an AHB write directly followed by an AHB read. In this case, a single wait state is asserted.

When the AXI4 interface is selected, the SRAM controller provides zero-wait-state AXI4 access to the synchronous SRAM in all cases except in case when both AXI read and AXI write channel are active at the same time. In that case AXI write transfer is delayed.

When the APB interface is selected, the SRAM controller provides low latency APB access to the synchronous SRAM in all cases. APB write and read transfers are completed in two clock cycles.

The SRAM-CTRL core is rigorously verified, silicon-proven and available in RTL source or as a targeted FPGA netlist.

Applications

The SRAM-CTRL core can be used in any SoC design, where a processor or some other module with an AHB, AXI or APB master interfaces needs to access one or more on-chip SRAMs.

Block Diagram
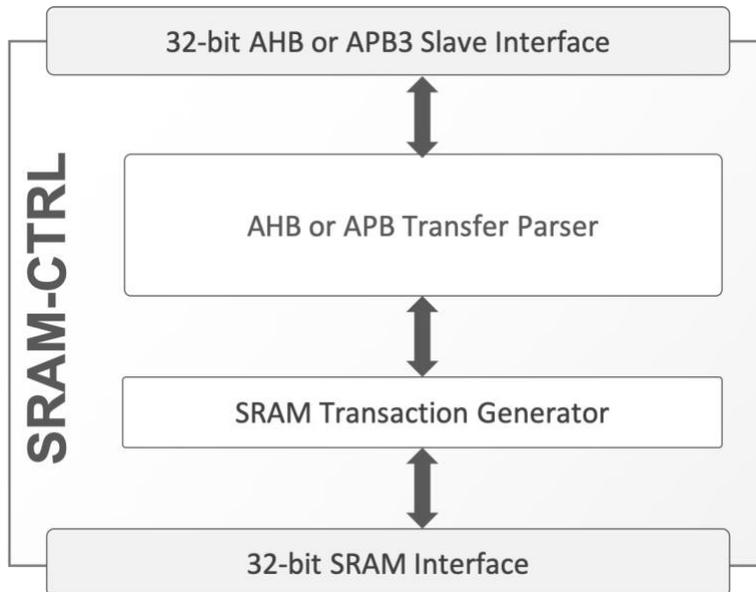
Support

The SRAM-CTRL as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.