ECC-SRAM

Error Correcting Code for SRAMs

The ECC-SRAM core adds protection against SRAM data corruption. It uses Error-Correcting Code (ECC) to implement single-bit error correction and double-bit error detection (SECDEC).

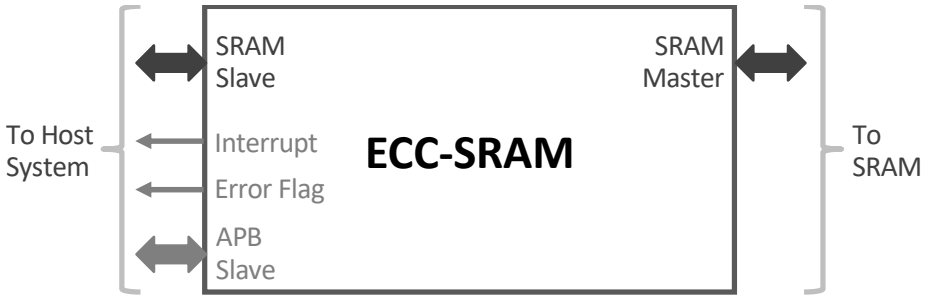
The core can be used to protect memories having a data-width with an integer multiple of 8-bits and not larger than 256 bits. It can optionally support partial word writes (e.g. write only one byte out of a 64-bit word), by automatically reading, modifying, and writing back the full word in order to properly update the stored ECC bits.

The core connects between an SRAM and the bus accessing it. Using the core in existing systems that were not originally designed with SRAM protection is straightforward, as the core detects and corrects errors without increasing the SRAM access latency. Using the ECC core increase the access delay of the protected SRAM, but this penalty is relatively small, thanks to the ECC-SRAM's highly optimized data-path. This delay overhead can be further reduced by using separate ECC-SRAM cores to protect different parts of the full word-width (e.g. use two cores each protecting 64 bits of a 128-bit memory).

The control and status registers for the core are accessible via a 32-bit APB interface. The occurrence and type (single-bit or double-bit) of an error is signaled to the system via a two-bit level-triggered interrupt line. A single-bit edge-triggered error indication interrupt is also provided by the core. The type and address of the last error are reported in the core's status registers, which the system may use for repairing or prohibiting access to the corrupted memory location. The use of the interrupt lines and registers enables the system to react in case of an error, but their use is optional; the core would operate even if the system chooses to ignore the interrupt lines and never access the APB interface.

The ECC-SRAM core is production-proven, rigorously verified, and available in RTL source or as a targeted FPGA netlist. Its deliverable includes a testbench, synthesis, and simulation scripts, instantiation examples and comprehensive user documentation.

Block Diagram



FEATURES

Error Correction

- Corrects any single bit error
- Optionally implements double bit error detection (SECDED)
- Optional Read-Modify-Write performed for writes of non-full-word size accesses
- Configurable length of protected data: Integer multiple of 8 and up to 256-bits

Easy Integration

- Error occurrence signalled:
  - As synchronous bus errors; and/or
  - As asynchronous interrupts; and/or
  - As a H/W flag for use in system control
- Location and type of errors reported in registers
- Control and Status registers accessible via APB
- Generic memory interfaces, easy to use with any standard SRAM module
- Zero-cycle error detection and correction. Core does not alter the access latency of the protected memory
- Fast, optimised logic minimizes additional SRAM access delay

Deliverables

- Synthesizable Verilog RTL
- Testbench & sample test cases
- Simulation & synthesis scripts
- Instantiation examples
- Documentation

Support

The ECC-SRAM as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.