Talos-BA2x

Talos Evaluation Kits for BA2x Processor IP Cores

The Talos-BA2x series of integrated hardware/software kits include everything you need to quickly and easily evaluate a BA2x Embedded Processor IP core in your own environment.

The evaluation kits are built on the versatile Terasic DE0-Nano Development and Education board, which uses an Intel Cyclone® IV 4C22 FPGA. The DE0-Nano board is delivered preconfigured with a BA2x Embedded Processor IP core.

Users can choose from representative BA2x embedded processors and the peripherals that are connected to it. In all cases a 64kB Quick Access Memory is attached to the BA2x



processor. Off-the-shelf configurations include UART, GPIO, I2C and SPI interface controllers; and a watchdog timer. These are connected to the processor via an AMBA bus fabric (i.e. AHB or AXI interconnect and a bridge to APB bus). Different peripheral configurations can be made available upon request.



Part of the evaluation kit is the extended GNU C/C++ toolset (i.e. GCC & GDB) for the BA2 processor, ported libraries and FreeRTOS example, all packaged and available under the Eclipse-based Beyond Studio[™] integrated development environment (IDE). A Beyond Debug Key supporting the IEEE 1149.1 and IEEE 1149.7 standard JTAG signal set—plus proprietary One-Wire Debug and Two-Wire Debug protocols—is also included in the Talos-BA2x evaluation kit.

A Talos-BA2x kit allows users to run their own performance, power, or code benchmarks, interface the processor with their own hardware system, and fully exercise and evaluate the processor to determine how well it will satisfy their specific project requirements.

About BA2x Embedded Processor IP Cores

The BA2x Embedded Processor cores are silicon-proven, royalty-free, easy to program, and technically competitive with traditional 32-bit processor choices. They all implement the variable length BA2[™] instruction set architecture which yields extremely dense code. This extreme code density helps reduce memory and cache sizes, enables fewer operations and longer sleep times, and cuts system-level energy consumption.

The family includes processors using one to five pipeline stages, which can be equipped with hardware multiplier, divider, multiply-accumulate, or floating-point units. These can be delivered pre-integrated with the customer's choice of bus fabric and peripherals.

Software development is facilitated by the Eclipse-based Beyond Studio IDE and a rich ecosystem of ported libraries, operating systems, and development boards.

BA2x embedded processors have been production proven since 2009 in numerous ASICs and SoCs for the consumer electronics, automotive, network and defense markets from tier-1 and smaller companies,

FEATURES

Complete Evaluation Kits

- A DE0-Nano Terasic board preconfigured with the BA2x Embedded Processor IP of your choice
- A Beyond Debug Key
 - Supports JTAG and proprietary single-wire or dual-wire debug interfaces.
- Eclipse-based Beyond Studio IDE
 - GNU C/C++ Toolset
 - Ported Libraries
 - Example FreeRTOS application
- Complete IP core and Evaluation Kit documentation

Versions

- Talos-BA2 Evaluation Kits are available for the following BA2x IP cores:
 - BA20 PipelineZero[™] 32-bit Embedded Processor, an ultralow-power processor using zero pipeline stages for instruction execution to provide maximum energy and performance efficiency.
 - BA21 32-bit Low-Power Deeply Embedded Processor, a dualpipeline low-power processor that delivers better performance than most processors its size.
 - BA22-DE 32-bit Deeply Embedded Processor, a flexibleand efficient processor with 4- or 5 pipeline stages that delivers the processing power required for demanding deeply embedded applications.
- Off-the-shelf configurations of the BA20, BA21, and BA22-DE cores use:
 - 64kB of unified QMEM memory
- Hardware multiplier
- Hardware divider
- Floating Point Unit (BA22 only)
- Programmable Interrupt Controller
- Tick timer
- AHB or AXI interconnect with a bridge to APB, and the following peripherals: UART, GPIO, SPI, I2C and Watchdog Timer

