H264-E-HIS

H.264 High 10 Intra Profile Encoder Core

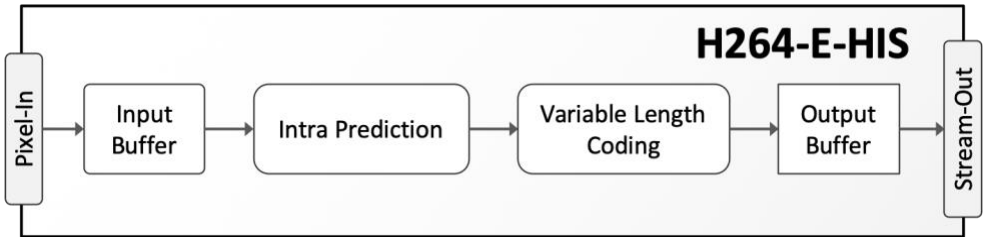
The H264-E-HIS IP core is a video encoder compliant to the High 10 Intra profile of the ISO/IEC 14496-10/ITU-T H.264 standard. The encoder core has a small silicon footprint—approximately 220K gates and 280K to 420K bits of SRAM—and requires no external memory (e.g. off-chip DRAM) allowing for very cost-effective and low-power ASIC or FPGA implementations.

Despite its small size, the H264-E-HIS implements a highly efficient intra-frame compression engine. When measured at the same bit rate, the video quality of the compressed streams it produces exceeds that of Motion-JPEG and is similar to or better than the video quality of Motion JPEG2000. Being intra-coded, the produced H.264 streams feature high error resilience, allow for random access in the compressed stream, and ease video editing. Furthermore, the core can output both Variable Bit-Rate (VBR) and Constant Bit-Rate (CBR) video. The core autonomously produces VBR streams, while CBR streams can be produced when quantization is externally adjusted on frame boundaries.

The core was designed for ease of use and integration. Once initially programmed, it compresses an arbitrary number of frames without any assistance from the host processor. Moreover, the core does not require any external memory (such as an off-chip DRAM) for its operation, and features FIFO-like flow-controllable interfaces for the pixel and compressed stream data. The core is optionally delivered with a raster-to-block converter, and bridges to AXI-Stream or Avalon Streaming interfaces.

Customers can further decrease their time to market by using CAST's integration services to receive complete video encoding subsystems. These integrate the encoder core with video and networking interface controllers, networking stacks, or other CAST or third-party IP cores.

Block Diagram



FEATURES

Compact, low-power AVC/H.264 encoder, suitable for applications requiring moderate-levels of compression

Encoding Features

- High 10 Intra profile with CAVLC entropy coding
- All 4x4 and 16x16 intra prediction modes except plane prediction
- 8-bit and 10-bit color depth and 4:2:0 chroma sampling format
- VBR: Variable Bit-Rate encoding with a fixed quantization parameter (QP)
- CBR – Constant Bit-Rate encoding with external adjustment of QP at frame boundaries

Ease of Integration

- Zero CPU overhead, stand-alone operation for VBR mode
- Requires no external, off-chip memory
- FIFO-like pixel-in and stream-out interfaces, optionally bridged to AXI-Stream or Avalon Streaming
- Optionally delivered with raster-to-block converter module

Performance and Size

- 2.35 clock cycles per pixel
- Up to UHD/4K in ASICs; and up to Full-HD in FPGAs
- 220k eq. Gates, and 280K to 420k bits of SRAM (depending on configuration)

Compression Efficiency

- Better than (Motion) JPEG, equivalent to, or better than (Motion) JPEG200

Silicon Resources Utilization

The H264-E-HIS can be mapped to any ASIC Technology (provided sufficient silicon resources are available) and optimized to suit the particular project's requirements. The following table provides sample implementation data for the core's default configuration. Note that these sample implementation figures do not represent the highest speed or smallest area possible for the core. Please contact CAST to get characterization data for your target configuration and technology.

Technology	Logic	Memory	Freq.	Throughput	Video Format
TSMC 26 HPM	100k um2 220k Gates	420K bits	600 MHz	255 Mpixels/sec	UHD/4k@30fps
TSMC-40G	216k um2 300k Gates	420K bits	600 MHz	255 Mpixels/sec	UHD/4k@30fps

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Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The H264-E-HIS IP core is available in source-code VHDL or as a targeted netlist. Its deliverables include a sophisticated self-checking testbench, sample synthesis and simulation scripts, a software (Bit-Accurate) model, and comprehensive user documentation.

H.264 Cores Family

The H264-E-HIS is one member of the family of H.264 cores that CAST offers. The following tables summarize the family's encoders and decoders and highlight the cores' basic features.

H.264 Encoder Cores	**H264-E-BIS** Intra-Only Baseline Profile	**H264-E-BPS** Low-Power Baseline Profile	**H264-E-MPS** Low-Power Main Profile	**H264-E-CFS** Ultra-Low-Power Baseline Profile	**H264-E-HIS** Intra-Only High Profile	**H264-E-BPF** Ultra-Fast Baseline Profile
Cycles/Pixel	4	4	4	4	2.5	2 or 1
Silicon Resources *	Very Small	Small	Small	Small	Moderate	Moderate-High
Profile	Constrained Baseline	Constrained Baseline	Main	Constrained Baseline	High 10 Intra	Constrained Baseline
Slices Types	IDR	IDR, P	IDR, P	IDR, P	IDR	IDR, P
Chroma Formats	4:2:0	4:2:0	4:2:0	4:2:0	4:2:0	4:2:0
Bits per sample	8	8	8	8	8, 10	8
Progressive/Interlaced	✓ / ✓	✓ / ✓	✓ / ✗	✓ / ✗	✓ / ✗	✓ / ✓
Multiple video channels	Optional	Optional	Optional	Optional	✗	Optional
CAVLC / CABAC	✓ / ✗	✓ / ✗	✗ / ✓	✓ / ✗	✓ / ✗	✓ / ✗
CBR and VBR	✓	✓	✓	✓	✗	✓
Intra-Refresh	N/A	✓	✓	✓	N/A	✓
Multiple Slices	✓	✓	✓	✓	✗	✓
Compressed Frame Store	✗	✗	✗	✓	N/A	N/A

* Very Small <100k Gates, Small < 200k Gates, Moderate < 500K Gates, and High > 500KGates

H.264 Decoder Cores	**H264-D-BP** Low Latency Baseline Profile Decoder	**H264-LD-BP** Low Power Baseline Profile Decoder
Profile	Constrained Baseline	Constrained Baseline
Profile Compatibility	Full	Limited to streams from the H264-E-BPS/BPF, BIS cores
Additional Features	✗	Interlaced with Main Profile Syntax
Throughput (cycles/pixel)	2.5	4
Silicon Resources	Moderate	Small

* Very Small <100k Gates, Moderate < 500K Gates

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