xSPI-MC

xSPI, HyperBus™, & Xccela™ Serial Memory Controller

The xSPI-MC core is a versatile serial/SPI memory controller, which allows a system to easily detect and access the attached memory device or directly boot from it. The controller core supports most of the proprietary SPI protocols used by Flash and PSRAM device vendors and is compatible to JEDEC's eXpanded SPI (xSPI), HyperBus™ and Xccela™ standards.

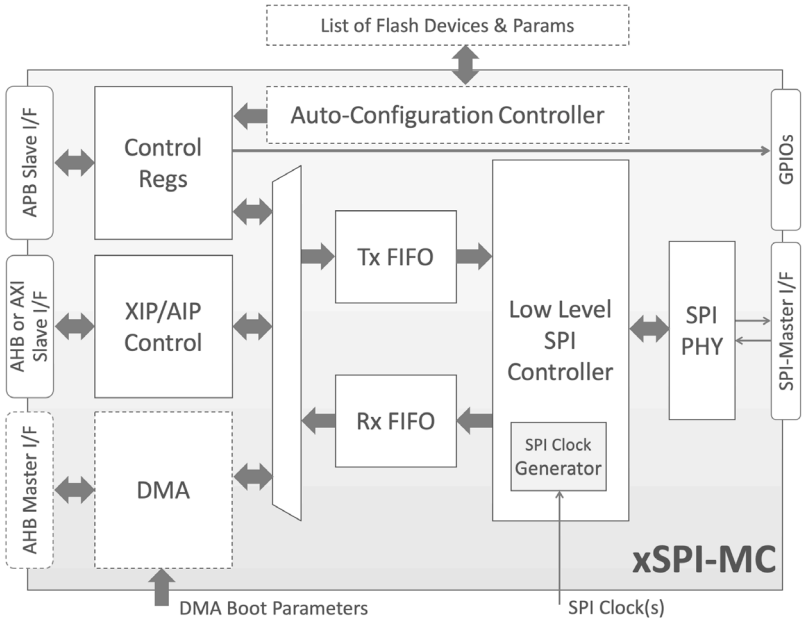
The core allows the system to interface with one or more serial memory devices in one of the following modes: a) in Slave mode by accessing its registers via an AHB slave interface, b) in DMA mode where the system programs the internal DMA engine, and then the core accordingly drives its AHB master interface, c) in Access In-Place (AIP) mode where the core allows the system to directly access the SPI memory address space via an AHB or AXI slave interface, d) in Boot-Image copy mode where after reset the core will autonomously copy an amount of data (boot-image) from the SPI memory to the AHB address space (e.g. on a shadow RAM, or DRAM) using its AHB master interface.

This memory controller can work with single, dual, quad, twin-quad, octal or 16x SPI memory devices. To enable use with memory devices from different vendors, the core offers two ways of configuring the device-specific parameters: a) via registers, where the system is responsible to identify the connected flash device and program the appropriate values to the core's registers, and b) by using the auto-configuration feature, where the core will autonomously identify the connected memory device and program itself accordingly. The auto-configuration functionality uses a user-provided memory that stores a list of automatically identifiable devices along with their features.

The xSPI-MC can be easily configured to match different application requirements. The instantiation of the DMA engine and the auto-configuration logic, the maximum number of memory devices that the core supports, and the reset values for all configuration registers, are some of the design parameters that can be controlled by means of simple Verilog defines.

The core can be implemented in any ASIC or FPGA technology, as it is delivered with a synthesizable soft-PHY and does not use any process-specific modules. Sample timing constraints are provided with the core and optional technology mapping support is available.

Block Diagram



FEATURES

SPI Memory Controller

- Supports xSPI (JEDEC's JESD251), HyperBus™, Xccela™ protocols and most proprietary SPI memory interfaces
- Works with Serial NOR, NAND, PSRAM and HyperRAM™ memory devices

Flexible Access Modes

- AIP/XIP – Enables read (XIP) or read and write (AIP) directly from the serial memory with zero software overhead
- DMA – Optional DMA for data transfer from/to system to/from the serial memory
- Boot-Image Copy – Autonomously copies data from the serial memory to the address space
- Slave Mode – System accesses core registers to transfer data to/from the serial memory

Easy Configuration

- Run-time SPI protocol programmable parameters:
  - Single, Dual, Quad, Twin-Quad, Octal and 16x SPI lanes
  - Single and Dual Transfer Rate
  - Bit-length and number of SPI lanes used for command, address
  - Latency and bus turn-around time
- Multiple programming options:
  - Auto-configuration
  - At run time
  - At synthesis time

Process-Independent Soft PHY

- Synthesizable, soft PHY and sample timing constraints included
- Optional technology mapping support is available

Safety-Enhanced Version (Optional)

- ISO26262 ASIL-B/C/D dependent on core configuration
- Nine ASIL-ready certified configurations

Versions and Configuration Options

The xSPI-MC is a highly configurable core and it is available in the configurations below. The Safety-Enhanced versions of the core implement spatial redundancy and CRC protected configuration data for protecting the inner logic of the core.

Version Name	xSPI-MC-Q(uad)	xSPI-MC-F(ull)
AHB Slave I/F	✓	✓
AXI Slave Interface	✓	✓
XIP (transparent read access)	✓	✓
AIP (transparent read/write access)	✗	✓
XIP Interrupts (Suspend/Resume) a Write or Erase Operation issued via the CSRs	✓	✓
Address-based CS	✓	✓
Sampling point adjustment per CS	✓	✓
Clock divider per CS	✓	✓
Prefetch	O	✓
AHB Master (DMA)	O	O
AutoBoot (Required DMA)	O	O
Autoconfig	O	O
PHY #1: Non-DQS, x2 (or higher) SPI Clock	✓	✓
PHY #2: DQS, x2 (or higher) SPI Clock	✗	✓
PHY #3: DQS, x1 SPI Clock	✗	O
PHY Option: Shifted clocks	O	O
Protocols Support (Use & Support limited to the supported protocols)		
xSPI	✓	✓
Hyperbus	✗	✓
Xccela	✓[4]	✓
Legacy & Proprietary[1]	✓	✓
Performance Options		
x1/x2/x4	✓	✓
x8/x16	✗	✓
DDR	✓	✓
Devices Support (Use & Support limited to the supported device types)		
Serial NOR	✓	✓
PSRAM	✓	✓
Serial NAND[2]	✗	O
Other[3]	✗	O
ISO26262 ASIL-B/C Version	O	O
ISO26262 ASIL-D Version	✗	O

Symbols Index
- ✓: Supported
- ✗: Not Supported
- O: Optionally Supported

Notes:

1. A set of legacy and proprietary protocols are verified to work with the core. More can be added on request.
2. Wear leveling / bad block management in customer software.
3. Other memory types may be added on request.
4. Limited to x1/x2/x4

Size and Performance

The xSPI-MC can be mapped to any ASIC or FPGA (provided sufficient silicon resources are available). Under its minimum configuration (XIP, no AIP, no DMA, no Auto-configuration) the core is about 12,000 gates. The speed of the SPI interface is process and configuration dependent. Please contact CAST to get accurate characterization data for your target technology and configuration.

Verification

The core and it's soft PHY has been verified and proven in production in various configurations and with several memory devices. Please contact CAST to learn more about your target configuration and memory devices.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty consecutive days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Support for technology mapping of the Soft PHY, if required, is also optionally available.

Deliverables

The core is available in synthesizable Verilog and FPGA netlist forms and includes everything required for successful implementation including a sophisticated Verilog testbench and user documentations. The optional safety-enhanced versions include the Safety Manual (SAM), a Failure Modes, Effects and Diagnostics Analysis (FMEDA) and the ASIL-D Ready certificate, issued by SGS-TÜV Saar GmbH.