WDT-APB

Watchdog Timer with APB Interface

The WDT-APB core implements 32-bit count down counter with a programmable timeout interval and logic to generate an interrupt and a reset signal on its timeout. The main purpose of the Watchdog IP Core is to trigger a system reset in case of software failure to prevent a system lock-up.

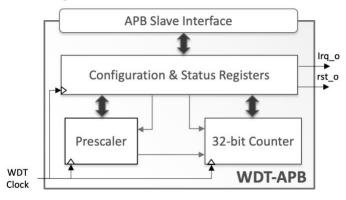
Via a 32-bit APB interface, the host processor can choose the timeout interval, enable, disable or clear the interrupt and reset lines, and pause or resume the timer. If the counter is enabled, it will decrement on every clock cycle. When the counter reaches zero, the interrupt output is asserted and the counter is reloaded with the timeout value. In case that the interrupt is not cleared before the counter reaches the zero value again, the output reset signal is asserted.

The core is designed so that the timer and the APB interface operate on different and unrelated clocks. This allows the timer to operate even when the rest of the system is in a low-power mode and bus clocks are not running.

Furthermore, to protect from unintentional configurations, write access to the core's configuration registers is enabled only when a separate register, the "lock register", holds a specific magic value. An attempt to write the core's configuration registers while the core is locked (while the lock register does not hold the magic value) triggers a bus error.

The WDT-APB core is rigorously verified and available in RTL source or as a targeted FPGA netlist. Its deliverable includes a testbench, synthesis and simulation scripts and comprehensive user documentation.

Block Diagram



Support

The WDT-APB as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

FEATURES

- Programmable 32-bit Down Counter with 16-bit pre-scaler
- Interrupt generation on counter timeout
- Reset generation on counter timeout in case that interrupt was not serviced
- Locking mechanism to prevent nonintentional configuration
- Suspend mode to allow system debug and sleep modes
- 32-bit APB3 interface
- Independent APB and timer clocks

Deliverables

- Synthesizable RTL or FPGA netlist
- Testbench & sample test cases
- Simulation & synthesis scripts
- Documentation

