WDR

Low-Power, Low-Latency HDR/WDR Image Processor

The WDR core implements an efficient, flexible, low-power and low-latency High Dynamic Range (HDR) and Wide Dynamic Range (WDR) image processor that produces clear and sharp images under any lighting conditions.

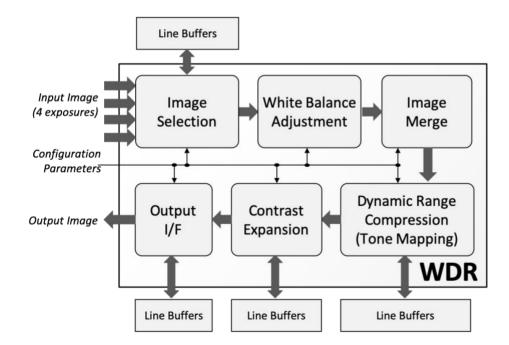
The core receives two, three, or four exposures of the same frame, in 10- or 12-bit RGB Bayer format and any resolution up to Full HD. It processes the input with proprietary, content-adaptive algorithms for merging exposures, tone mapping (local and global), and contrast expansion, and it also supports white balance adjustment, optical back correction, and a 2D reduction noise filter.

Being highly configurable and sensor-agnostic, the core can address the needs of a wide range of applications. Run-time control over processing parameters enables users to adjust brightness, dynamic range width, and sharpness to address the requirements of different use cases, and also provides the means to eliminate typical HDR/WDR processing artifacts such as flickering, shape deformation, and over-enhanced edges.

The WDR core requires only a few lines of buffering and adds minimal processing latency. It features extremely low power consumption due to the absence of a power-consuming frame buffer, which is typically implemented in external DDR memory.

The core is designed with industry best practices, and its reliability has been proven through both rigorous verification and mass production. Its deliverables include a complete verification environment and a bit-accurate software model.

Block Diagram



FEATURES

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Versatile and Efficient

- Content Adaptive Frame Merge
 - o Merges 2, 3 or 4 exposures
 - Programmable exposure times and speed of response to content changes
- Advanced Tone Mapping
 - Local & Global Tone mapping
 - Programmable contribution of local VS global tone mapping
- 2D Noise Reduction Filter and Contrast Expansion of Programmable Strength
- White Balancing Adjustment and Optical Black Correction
- Optional, customizable motionadaptive deghosting

Low Latency & Low Power

- No frame buffers; does not need power-consuming DDR
- Just seven lines of latency

Sensor-Agnostic and Tunable to Application Requirements

- User control over processing parameters allows tuning to specific application needs
- 2, 3 or 4 input exposures
- 10- or 12-bit per sample Raster-Scan Bayer RGB Input

Proven & Reliable

- Mass production proven
- Scan-ready, LINT-clean design

Deliverables

- Verilog RTL or targeted netlist
- Comprehensive documentation
- Testbench
- Bit-Accurate C Model
- Sample synthesis and simulation scripts





Applications

The core's efficiency makes it suitable for a wide range of applications using image sensors. Its low-latency processing makes it ideal for systems involving real-time human or machine interaction with the video content, such as those in automotive, industrial, medical, and several types of surveillance applications.

Size and Performance

The following table shows silicon resources utilization and performance information for different technology targets, with the core configured to support Full-HD resolution. These figures do not represent the smallest area or higher processing rate that may be achieved. Please contact CAST to get area and performance characterization information for your specific requirements.

Target Technology	Silicon Resources	Performance
TSMC 28nm (hpm- sc9-svt-c31)	560K Gates and 980K bit of SRAMs	1080p120
Xilinx⊚ Artix⊚-7, Kintex⊚-7, Kintex⊚ Ultrascale™	40K LUTs, 43 Block RAM Tiles, 91 DSPs	1080p60 on Kintex UltraScale 1080p30 on Artix- 7 and Kintex-7
Intel® Arria® 10, Stratix® V	30K ALMs, 80 RAM Blocks, 91 DSP Blocks	1080p60 on Stratix V 108p30 on Arria 10

