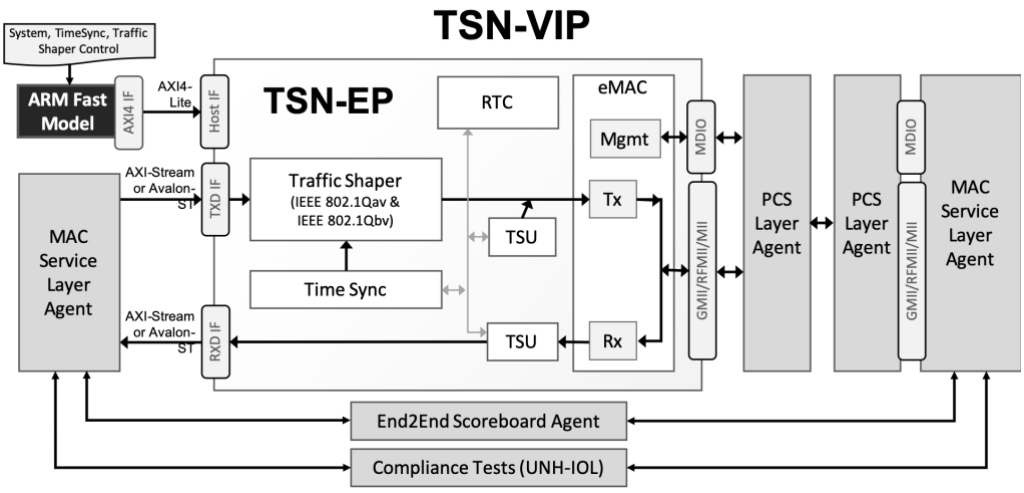
TSN-VIP

TSN Ethernet Verification IP

The TSN-VIP Ethernet Verification IP package provides a complete, simulation-based functional verification solution for design levels from the TSN-EP TSN Ethernet End Point Controller core through a complete SoC.

TSN-VIP includes MAC and PHY models, protocol checking, and an optional compliance testsuite based on the UNH-IOL test specifications. Its integration with the ARM® Fast Model integration enables running the TSN-EP software stack in one fully integrated testbench.

Block Diagram



Specification Conformance

The TSN-VIP package supports these key TSN IEEE 802.1 and 802.3 specifications:

- Peer delay mechanism (wIEEE 1588 PTP)
- Scheduled traffic (802.1Qbv)
- Frame preemption (802.3br and 802.1Qbu)
- Credit based shaper (802.1Qav)
- Cyclic queuing and forwarding (802.1Qch)
- Per-stream filtering and policing (802.1Qci)
- Time synchronization (802.1AS)
- Frame replication and elimination (802.1CB)
- Stream reservation (P802.1Qcc/D2.3)
- Stream reservation Protocol(802.1Qat)
- Asynchronous traffic shaping (P802.1Qcr/D0.5)

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core includes
everything required for successful implementation:

- SystemVerilog/UVM agents for MAC and PHY\
- Testbenches including Avery Design VIP-based
- Optional ARM Fast Model integration & debug environment
- Optional compliance testsuite including UNH-IOL tests
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation

FEATURES

- Modular multi-port MAC and PHY models
  - MAC Control, Status, & Service Registers
  - MDIO support
  - MAC Service layer
- PHY-level PCS/PMA layer models
  - 10/100M, 1/10/25/40/50/100/200/400 Gbps
  - Supports AUI, serdes interfaces
  - Multiple FECs
  - NRZ and PAM-4 signaling
  - Auto-negotiation
  - Link Training
  - Pause operation
  - Programmable inter-frame gap timing
- Supports key TSN IEEE 802.1 and 802.3 specifications (see text)
- Additional MAC Service layer features
  - Tagged Frames support
  - Priority-based Flow Control (PFC)
  - Enhanced Transmission Selection (ETS)
  - Data Center Bridging eXchange (DCBX)
- SystemVerilog/UVM models and testsuites
- Timing class to models clocking, skews, min/max timing
- Runtime configurable architecture including speed, number of lanes, FEC, Alignment Marker Dist
- Callbacks at all levels including error frame, length, SFD, FCS, IPG, FEC injection capabilities
- MAC, PCS, FEC, and AN protocol tracker logs
- Built-in protocol checkers and coverage reports
- Performance metrics: effective line rate, active/pause modes
- UNH-based Compliance testsuite targets exercising protocol checklist items

CAST

www.cast-inc.com • info@cast-inc.com • tel +1 201.391.8300

Sourced from avery design systems