TSN-SW

Multiport TSN Ethernet Switch

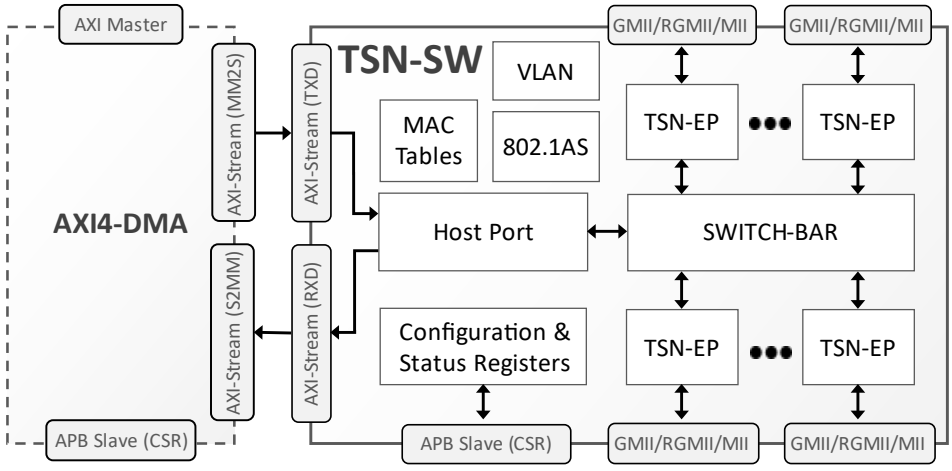
The TSN-SW implements a highly flexible, low-latency, multiport TSN Ethernet switch. It supports the hardware functionality for Ethernet bridging according to the IEEE 802.1Q standard and implements the essential TSN timing synchronization and traffic-shaping protocols (i.e. IEEE 802.1AS-2020, 802.1Qav, 802.1Qbv, and 802.1Qbu, 802.1br). Enhanced reliability features can also be supported, using the optional hardware modules for Frame Replication and Elimination for Reliability (IEEE 802.1CB) and Per-Stream Filtering and Policing (IEEE 802.1Qci). Featuring a configurable number of ports, the Layer-2 switch operates in cut-through mode at wire speed and can provide sub-microsecond port-to-port latency. The core is hence suitable for applications with demanding real-time requirements.

The TSN-SW operates efficiently under different usage scenarios and is highly configurable. Users can configure key factors via the core's control registers: the mapping of VLAN priority levels to TSN traffic classes, the traffic scheduling and preemption parameters, the treatment of special frames (i.e. broadcast, unknown, & internal), as well as the VLAN ID and MAC lookup tables used for frame forwarding and filtering. The host system can also switch the mode of operation of each individual port from cut-through to store-and-forward to eliminate the propagation of bad frames at the cost of increased latency. The core otherwise operates autonomously and only requires software assistance at runtime for correct time synchronization; a lightweight ptp/802.1AS software stack comes with the core for that purpose.

The TSN-SW uses standard AMBA® interfaces to ease integration. Its control and status registers are accessible via a 32-bit-wide APB bus, and packet data can be exchanged with the host system via AXI-Streaming interfaces with 32-bit data buses. To further expedite and ease the implementation of customer applications, DMA engines providing access to the stream interfaces via a memory-mapped AXI4 master port, and software stacks supporting higher-layer protocols, such as IEEE 802.1Qcc, IEEE 802.1Qca and SNMP, are optionally available.

The TSN-SW is designed with industry best practices and is available in synthesizable RTL (Verilog 2001) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample synthesis and simulation scripts, an extensive testbench, and comprehensive documentation.

Block Diagram



FEATURES

Low-Latency & Flexible Switch

- Configurable number of 3 to 24 full-duplex Ethernet ports plus one internal port
- Low-latency cut-through or robust store-and-forward mode selectable per port
- Sub-microsecond port-to-port latency, in cut-through mode
- 10/100/1000 Mbps (10Gbps soon)
- 802.1Q Tagged VLAN support
- Port-based VLAN
- Configurable VLAN-PCP to TSN-queue mapping (QoS by PCP)
- Flexible VLAN and MAC forwarding & filtering
- Configurable VLAN-ID & MAC lookup table for dynamic and static entries
- Automatic aging table
- Untagged ports support
- Port Statistics
- Port mirroring

TSN Features

- IEEE 802.1AS-2020 (requires lightweight software PTP stack)
- Traffic shaping per IEEE 802.1Qav & IEEE 802.1Qbv with eight TSN-Queues
- Frame preemption per IEEE 802.1Qbu and IEEE 802.3br
- Frame Replication and Elimination per IEEE 802.1CB and Per-Stream Filtering and Policing per IEEE 802.1Qci (optionally implemented in hardware)
- Path Control and Reservation per IEEE 802.1Qca, and Enhancements to Stream Reservation Protocol per EEE 802.1Qcc (optionally implemented in software)

Easy System Integration

- AMBA® SoC Interfaces
  - 32-bit APB for register access
  - 32-bit AXI4-Stream for packet data
  - Optional AXI4 DMA engine
- MII, GMII or RGMII, and MDIO Ethernet PHY interface per port
- Requires minimal host assistance for initialization and operation
- Provides a wide range of statistics via optionally instantiated counters
- Complete FPGA reference designs available

Applications

The TSN-SW is suitable for implementing TSN Ethernet End-points in daisy-chained networks (e.g. ring topologies) requiring robust, low-latency, and deterministic communication. Such networks are used in automotive, industrial control, medical, and aerospace applications.

Implementation Results

The TSN-SW can be mapped to any AMD FPGA device (provided sufficient silicon resources are available). The FPGA resources requirements depend on the core configuration. The following are sample results for a typical core configuration. Please contact CAST to get characterization data for your target configuration and technology.

Family/Device	Configuration*	Logic	Memory
Zynq UltraScale+ zu9eg-2-e	4 ports 128 Lookup Entries 2kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth Frame Preemption	41,999 LUTs	65 RAMB36 28 RAMB18
Kintex 7 7k160t-1	4 ports 128 Lookup Entries 2kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth Frame Preemption	42,650 LUTs	65 RAMB36 28 RAMB18
Kintex UltraScale ku115-2-I	4 ports 128 Lookup Entries 2kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth Frame Preemption	42,330 LUTs	65 RAMB36 17 RAMB18
Kintex UltraScale+ ku15p-1-I	4 ports 128 Lookup Entries 2kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth Frame Preemption	42,330 LUTs	65 RAMB36 17 RAMB18
Kintex UltraScale+ ku115p-2-I	15 ports 128 Lookup Entries 2kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth Frame Preemption	149,911 LUTs	186 RAMB36 61 RAMB18

*Partial list of configuration parameters

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The TSN-SW has been rigorously verified, hardware-validated, and proven in real-life environments.

It has also been tested and verified at TSN interoperability plugfests organized by the Labs Network Industry 4.0 (LNI 4.0) association and the Industrial Internet Consortium (IIC).

Deliverables

The core includes everything required for successful implementation:

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation
- Lightweight PTP stack, easily portable to any other RTOS

Reference FPGA designs with a freeRTOS example software stack with Command Line Interface can be made available on request.

Related Products

The core is a member of CAST's family of automotive interface products that includes:

- TSN-EP TSN Ethernet Endpoint IP Core
- TSN-SE: TSN Ethernet Switched Endpoint IP Core
- LLEMAC-1G Low-Latency 10/100/1000 Ethernet MAC IP core
- CAN 2.0/CAN FD/CAN XL Controller IP core
- LIN 2.2/2.1/2.0 Master/Slave Controller IP core
- SENT/SAE J2716 Transmitter/Receiver Controller IP core

The TSN-SW can be easily integrated with the following IP cores also available from CAST:

- AXI4 DMA engine
- AXI4 Scatter-Gather DMA engine
- UDP/IP 1G/10G Hardware Protocol Stack
- TCP/UDP/IP 1G/10G Hardware Protocol Stack