TSN-SE

TSN Ethernet Switched Endpoint Controller

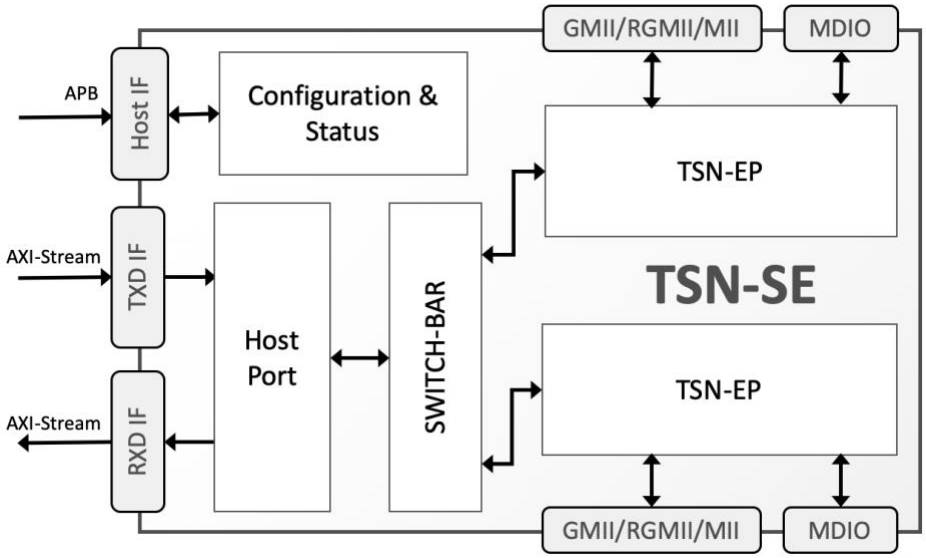
The TSN-SE implements a configurable controller meant to ease the implementation of switched endpoints for Time Sensitive Networking (TSN) Ethernet networks. It integrates hardware stacks for timing synchronization (IEEE 802.1AS), traffic shaping (IEEE 802.1Qav and IEEE 802.1Qbv), frame-preemption (IEEE 802.1Qbu and IEEE 802.3br) and a low-latency Ethernet MAC.

The controller core is designed to enable high-precision timing synchronization and flexible yet accurate traffic scheduling. With cut-through switching and minimal buffering even at the Ethernet MAC level, the TSN-SE features extremely low and deterministic ingress and egress latencies, and simplifies the development of time-aware applications. Furthermore, it allows the system to define and tune in real time the traffic shaping parameters according to an application's requirements, and pro-vides the system with timing information (time-stamps, alarms, etc.) that is typically required for the operation of a TSN network bridge or endpoint.

The TSN-SE uses standard AMBA® interfaces to ease integration. Its configuration and status registers are accessible via a 32-bit-wide APB bus, and packet data are input and output via AXI-Streaming interfaces with 32-bit data buses.

The TSN-SE is designed with industry best practices, and is available in synthesizable RTL (Verilog 2001) source code or as a targeted FPGA netlist. Deliverables provide everything required for a successful implementation, including sample scripts, an extensive testbench, and comprehensive documentation.

Block Diagram



Applications

The TSN-SE is suitable for the implementation of TSN Ethernet Endpoints in daisy chained networks (e.g. ring topologies) requiring robust, low-latency, and deterministic communication. Such networks are used in automotive, industrial control, medical, and aerospace applications.

FEATURES

TSN Ethernet Switched Endpoint

- Two Ethernet ports & one host processor port
- Suitable for daisy-chained networks such as rings

Low Latency & Flexible Switching

- Low-latency Layer-2 Cut-Through Switching
- Run-time switch configuration enables fast response to network changes
- 802.1Q Tagged VLAN support
- Port-based VLAN
- Configurable VLAN-PCP to TSN-Queue Mapping (QoS by PCP)
- Flexible VLAN and MAC forwarding & filtering
- Configurable MAC lookup table for dynamic and static entries & automatic ageing table
- Untagged ports support

TSN Features

- Ready for IEEE 802.1as (light-weight software stack available)
- Traffic shaping per IEEE 802.1Qav & IEEE 802.1Qbv with eight TSN-Queues
- Frame preemption per IEEE 802.1Qbu and IEEE 802.3br
- IEEE 802-1AS-2020, 802.1CB, 802.1Qci & 802.1Qcc (coming soon)

Easy System Integration

- AMBA™/AXI4 SoC Interfaces
  - 32-bit APB control/status interface
  - 32-bit AXI4-Stream for packet data
- MII, GMII or RGMII, and MDIO Ethernet PHY interface per port
- Requires minimal host assistance for its initialization and operation
- Complete reference designs available for Altera and Xilinx, including lightweight PTP stack sample application software

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Implementation Results

The TSN-SE can be mapped to any Xilinx FPGA device (provided sufficient silicon resources are available). The FPGA resources requirements depend on the core configuration. The following are sample results for a small number of core configurations. Please contact CAST to get characterization data for your target configuration and technology.

Family/Device	Config.*	Logic	Memory
Kintex 7 XC7k325-2	64 Lookup Entries 16kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth No Frame Preemption	12,253 LUTs	30 RAMB36 22 RAMB18
Kintex 7 XC7k325-2	256 Lookup Entries 16kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth No Frame Preemption	14,922 LUTs	57 RAMB36 23 RAMB18
Kintex 7 XC7k325-2	256 Lookup Entries 16kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth No Frame Preemption	17,941 LUTs	64 RAMB36 31 RAMB18
Kintex UltraScale XCKU035-1-c	256 Lookup Entries 16kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth No Frame Preemption	17,320 LUTs	64 RAMB36 31 RAMB18
Kintex UltraScale+ XCKU3P-1-I	256 Lookup Entries 16kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth No Frame Preemption	18,262 LUTs	64 RAMB36 31 RAMB18
Kintex 7 XC7k70t-1	128 Lookup Entries 2kB Ingress Mem 4 Traffic Classes 1k TC Queue Depth Frame Preemption	23,533 LUTs	38 RAMB36 16 RAMB18
Kintex 7 XC7k70t-1	256 Lookup Entries 2kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth Frame Preemption	31,858 LUTs	91 RAMB36 25 RAMB18
Kintex UltraScale XCKU115-2-I	4k Lookup Entries 8kB Ingress Mem 8 Traffic Classes 1k TC Queue Depth Frame Preemption	78,176 LUTs	538 RAMB36 20 RAMB18

*Partial list of configuration parameters

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Verification

The TSN-SE has been rigorously verified, hardware-validated, and tested in real-life environments.

It has also been tested and verified at TSN interoperability plugfests organized by the Labs Network Industry 4.0 (LNI 4.0) association and the Industrial Internet Consortium (IIC).

Deliverables

The core includes everything required for successful implementation:

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample Simulation and Synthesis scripts
- Comprehensive Documentation
- Lightweight PTP stack
- Device driver for FreeRTOS and Linux,

Related Products

The core is a member of CAST's family of automotive interface products that includes:

- TSN-EP TSN Ethernet Endpoint IP Core
- TSN-SW: TSN Ethernet Switch IP Core
- TSN-VIP TSN Ethernet Verification IP
- LLEMAC-1G Low-Latency 10/100/1000 Ethernet MAC IP core
- CAN 2.0/CAN FD/CAN XL Controller IP core
- CAN 2.0/CAN-FD Verification IP
- LIN 2.2/2.1/2.0 Master/Slave Controller IP core
- SENT / SAE J2716 Transmitter/Receiver Controller IP core