Timer-APB

Timer/Counter with APB Interface

The Timer-APB core is a 32-bit counter/timer with an APB interface that can be used to schedule periodic tasks and can act as a high precision time reference.

The timer supports three modes of operation: One-shot, auto-restart and continuous. In one-shot mode the counter runs until it reaches a user-defined value and it is then automatically disabled. In auto-restart mode the counter will reset itself and continue counting after reaching a user-defined value. In continuous mode, the counter is free-running and no special action is taken by the core.

Furthermore, the core can generate an interrupt every time the counter reaches a user defined value. This allows the host to use the core to get one-time trigger at a time, or periodic triggers.

Via a 32-bit wide APB3 interface, the host processor can choose the operation mode, configure the interrupt-generation, pause or resume the timer, read or write the timer value, and program the prescaler.

The prescaler allows trading timer accuracy for a wider timer range. Without the use of the prescaler, the 32-bit counter can generate a trigger after or every 2^{32}-1 clock cycles. The prescaler allows to further extend this time period. The programmable prescaler value will determine the number of clock cycles after which the counter/timer will be incremented.

The core is designed so that the timer and the APB interface operate on different and unrelated clocks. Furthermore, the core provides two interrupt output signals: one synchronous to the APB clock and one synchronous the timer clock.

The Timer-APB core is rigorously verified and available in RTL source or as a targeted FPGA netlist. Its deliverable includes a testbench, synthesis and simulation scripts and comprehensive user documentation.

FEATURES

- 32-bit Timer/Counter
- 32-bit APB3 interface
- Independent APB and timer clocks
- Programmable prescaler (synthesis-time defined bit-width)
- One-shot, auto-restart and continuous operation modes
- Maskable Interrupt
  - Two interrupt outputs: one synchronous to the APB clock, and one synchronous to the timer clock
- Suitable to schedule OS and/or user tasks, or a high precision time reference

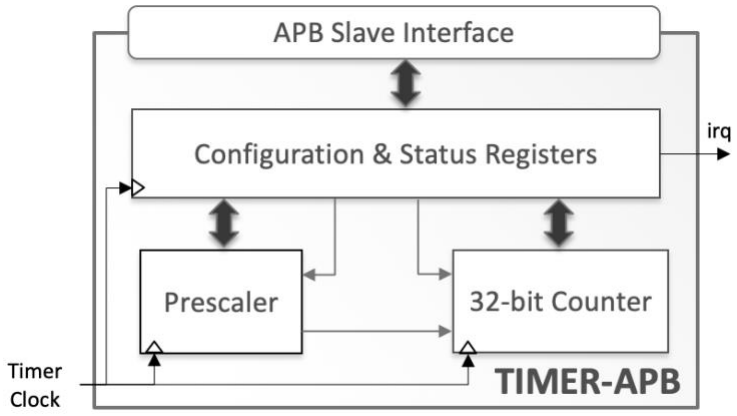
Deliverables

- Synthesizable RTL or FPGA netlist
- Testbench & sample test cases
- Simulation & synthesis scripts
- Documentation

Applications

The Timer-APB core can be used to provide periodic triggers and a time-base to Real-Time Operating Systems or software applications.

Block Diagram



Support

The Timer-APB as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.