CAST UDP/IP Hardware Protocol Stacks and Ethernet Link Speed

The CAST UDPIP core implements a UDP/IP hardware protocol stack that enables high-speed communication over an Ethernet Link. Besides the UDP and IPv4, there are also additional protocols implemented in the core (ARP/ICMP/IGMP/DHCP). The UDPIP core does not require processor assistance for its operation.

The Ethernet link speed depends on the Ethernet MAC layer implementation, which is not part of the UDPIP core, and therefore the UDPIP core does not have any control over the link speed. Although the UDPIP core does not depend on, nor it determines the Ethernet link speed, there are multiple versions of the UDPIP core named according to its recommended target speed:

- UDPIP-1G – stands for a 32-bit version of the UDPIP core datapath.
- UDPIP-10/25G – stands for a 64-bit version of the UDPIP core datapath.
- UDPIP-40/50G – stands for a 256-bit version of the UDPIP core datapath.
- UDPIP-100G – stands for a 512-bit version of the UDPIP core datapath.

The UDPIP-1G (32-bit datapath) allows supporting up to 1G (10M/100M/1000M) while running at 31.25MHz+ clock speed. The UDPIP-1G may support a 10G link if and only if it can run at 312.5MHz+ when mapped on the target technology. This is quite challenging in less powerful FPGAs or older ASIC technologies, so its use for the 10G link speed needs to be carefully analyzed.

The UDPIP-10/25G (64-bit datapath) allows support up to 10G while running at 156.25MHz+. The core can also support 25Gbps link speed in technologies where the 25Gbps+ transceivers are implemented and the core can achieve 390.625MHz system clock speed, such as Xilinx UltraScale+, Intel Stratix-10, and most of the modern ASIC technologies. The slower link speeds may also be supported but this usually requires a datapath width conversion to the typically narrower data interface of an 1G Ethernet MAC.

The UDPIP-40/50G (256-bit datapath) allows support of the 40Gbps link while running at 235MHz+. The core may support 50Gbps link speeds in the fast-enough technologies, such as Xilinx UltraScale+, Intel Stratix-10 and most of the modern ASIC technologies. The slower link speeds may be supported too but require a datapath width conversion to a narrower Ethernet MAC data interface.

The UDPIP-100G (512-bit datapath) supports 100Gbps link speed while running at 322MHz or faster system speed. The slower link speeds are supported too but require a datapath width conversion to a narrower Ethernet MAC data interface.

TABLE 1 T MAC DATA INTERFACE.A NARR

Core name	Data path	Required System Clock Speed [MHz]					
		1Gbps	10Gbps	25Gbps	40Gbps	50Gbps	100Gbps
UDPIP-1G	32-bit	31.25	312.5	X	X	X	X
UDPIP-10G/25G	64-bit	15.625	156.25	390.625	X	X	X
UDPIP-40G/50G	256-bit	-	60	147	235	292	X
UDPIP-100G	512-bit	-	-	-	156.25	195	322

The Ethernet MAC link speed switching (if possible and implemented) is outside the scope of the UDPIP core.