T8051XC3

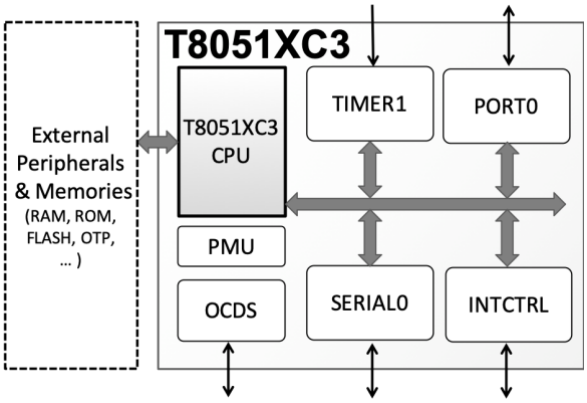
Ultra-Small 8051-Compatible Microcontroller

The T8051XC3 core implements one of the smallest-available 8-bit MCS®51-compatible microcontrollers. The core integrates an 8051 CPU with a serial communication controller, flexible timer/counter, multi-purpose I/O port, interrupt controller, and optionally with a debug unit supporting JTAG and Single-Wire interfaces.

The MCU executes some 8051 instructions in a single clock cycle, thus providing 0.1235 DMIPS/MHz (using the IAR Compiler) or 7.94x the performance per MHz of the original Intel 8051. Furthermore, the core can run at frequencies over 800MHz on a 40nm technology, offering performance that is almost 900x that of the original 8051.

The T8051XC3 runs the legacy code of existing systems, but is also ready for highly productive new software development. This is facilitated through CAST's on-chip debugging option, and debug pods that cooperate with the Keil µVision C51 and IAR Embedded Workbench for 8051 IDEs.

This T8051XC1 IP core builds on CAST's experience with hundreds of 8051 IP customers going back to 1997. It is rigorously verified, scan-ready, and available in source-code RTL or targeted FPGA netlist. The core is strictly synchronous, with positive-edge clocking (except in the optional module), synchronous/asynchronous reset (user-selectable), and no internal tri-states.



Applications

The T8051XC3 core is an ideal microcontroller for applications with strict area and power requirements. Its processing power is sufficient for controlling, calibrating, and preprocessing data from a wide range of MEMs, sensors, or analog front ends. It also provides an easily programmed alternative to hard-coded control logic (e.g FSMs).

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Sample Implementation Results

The following are sample ASIC pre-layout results and do not represent the absolute highest speed or smallest area possible. (Area figures do not include memories.)

	Technology	Clock Freq. (MHz)	Area (eq. Gates)
T8051XC3–CPU (CPU-only)	40nm	815	4,015
T8051XC3 (CPU, peripherals, no-OCDS)	40nm	815	6,582

FEATURES

- Fully compatible with the MCS®51 instruction set
- Compact silicon footprint:
  - CPU-Only: 4.0k Gates on 40nm
  - Complete MCU: 6.6k Gates on 40nm
- 0.1235 DMIPs/MHz or 7.94x more performance per MHz than the original Intel™ 8051 with the IAR compiler

Software Development

- Supported by IAR Embedded Workbench™ for 8051 and Keil µVision™ C51 IDEs
- JTAG-based or Single-Wire Serial Debug
- Compatible with any MCS®51 compiler

Interfaces and Peripherals

- Special Function Registers interface
- Up to 256B of internal data memory interface
- External memory Interface
  - Up to 64KB external program memory
  - Up to 64KB external data memory
- Interrupt Controller with two or four priority levels, and eight interrupt sources
- 8-bit Parallel I/O Port
- Serial 0 full-duplex serial (UART) interface
- Timer 1: Flexible timer/counter
- On-Chip Debug Support (OCDS)
- Power Management Unit with power-down modes (IDLE/STOP)
- Other peripherals and extensions available upon request

Deliverables

- Verilog RTL source code or FPGA netlist
- An example chip implementation, which uses the core in a sample system
- Sophisticated self-checking HDL Testbench
- Sample Simulation and Synthesis scripts
- Comprehensive documentation

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