T80251XC3

Tiny, Configurable 80251 Microcontroller

The T80251XC3 core implements a compact 16-bit microcontroller that executes the MCS®251 & MCS®51 instruction sets and includes a configurable range of features and integrated peripherals.

The core's advanced architectural design enables a high-performance 8051/80251-compatible MCU in a relatively small silicon footprint. The CPU itself (including the register files) is smaller than 15,600 gates, and can deliver 0.1455 DMIPS/MHz.

The T80251XC3 is extremely energy efficient, especially for applications that process 8- or 16-bit data. Its small footprint translates to very little power leakage, and its better performance than other 8-bit or 16-bit MCUs allows clocking at lower frequencies. Users can also adjust the core's energy consumption to match the processing workload via dynamic frequency scaling and independent control of the CPU and peripherals clocks. Finally, the 80251 ISA's complex addressing modes minimize the number of load/store operations, which typically comprise 20% or more of a RISC processor's code. With denser code needing smaller firmware memory and fewer required memory accesses, the energy consumption of the MCU's memory subsystem can be significantly less with the T80251XC3.

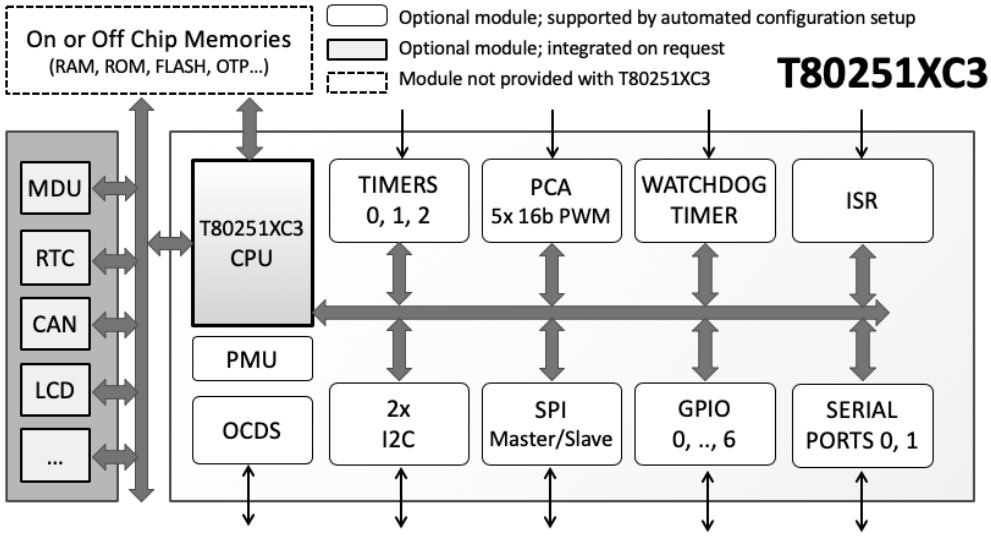
The core has a rich set of optional features and pre-integrated peripherals, allowing function, performance, and area to be balanced for each specific application. Software development is facilitated by a single-wire or JTAG debugging interface that operates seamlessly within the ARM® Keil® C251 integrated development environment. Inexpensive debug pods and a complete reference design board package are available.

This 80251 core builds on CAST's experience with hundreds of 8051 IP customers going back to 1997. Designed for easy reuse in ASICs or FPGAs, the core is strictly synchronous, with positive-edge clocking (except in the optional debug & SPI modules), synchronous or asynchronous reset, and no internal tri-states.

Applications

The T80251XC3 is a low-power and relatively inexpensive processor that can be used for a variety of tasks, for example as a peripheral microcontroller in complex SoCs, a sensor subsystem MCU in IoT applications, or an embedded processor in mixed-signal ICs.

Block Diagram



FEATURES

Fully compatible with the MCS®251 & MCS®51 instruction sets

Small Silicon Footprint

- CPU is below 13k gates on 180nm
- Smaller memory footprint, due to denser code for 8- and 16-bit data processing
  - ISA Addressing modes minimize load/store operation typically comprising 20%-25% with RISC CPUs

Energy Efficient

- Low leakage and static CPU power on the CPU, due to small silicon footprint
- Low energy for instruction and data transfers and storage due to addressing modes that minimizes the need for load/store operations
- Advanced power management supports dynamic frequency scaling and CPU and/or peripherals clock gating

Performance

- 0.1455 DMIPS/MHz for a 15.48x speed-up over the original 8051 at the same clock frequency
- Hundreds of times faster than the original 8051 when clocked at maximum frequency

Configurable Microcontroller

- Automatic instantiation of user selectable MCU peripherals
- Pre-integration with other CAST IP on request

Easy Firmware Development

- CDP-XC on-chip debug interface, supports JTAG and Single-Wire
- USB-to-Serial and USB-JTAG, low cost CDP-XC debug pods
- Seamless integration with Keil µVision™

Flexible Memory Architecture

- 16MB program and data address space; 64kB stack space
- Acknowledged transactions feature makes integration with slow memoires or peripherals easy
- 14x32-bit general purpose registers
- Up to 23 interrupts, with two or four interrupt priority levels

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Peripherals and Options

The T80251XC3 allows the user to easily select among a rich set of pre-integrated and pre-verified peripherals and core configuration options. Simple Verilog defines (e.g., “define USE_PMU”) are used for this purpose. The following list summarizes the peripherals and configuration options that are available. Those noted with an asterisk are not included by default with the T80251XC3, but can be added on request.

Timers/Counters

- **Timer 0 & 1**: 80C51-like 16-bit timers/counters
- **Timer 2**: 8052-like 16-bit counter
- **PCA**: 80251-like programmable counter array with five PWM channels
- **WDT**: 80251-like Watchdog Timer

Interfaces

- **I2C 0 & 1**: Master-Slave ports for Phillips Inter-Integrated Circuit (I2C) serial bus
- **SPI**: Master-Slave port for Serial Peripheral bus Interface serial bus
- **Serial 0**: 80C51 or 80251-like Full-Duplex UART/USART
- **GPIO 0-4**: 80C51-like 8-bit Input / Output parallel ports
- **SFR**: Special Function Registers interface
- **ISR**: 80251-like Interrupt Controller with up 23 sources, and two or four priority levels
- **GPIO 5***: 80C515-like parallel port 5
- **CAN***: Controller Area Network Bus 2.0 and Flexible Data (FD) Controller
- **LIN*:** Local Interconnect Network Bus Controller
- **OCDS**: On-chip debugging system interface

Performance Acceleration & Architectural Options

- **VDMA***: Direct Memory Access controller, with up to 8 channels
- **PMU:** Power management unit

Sample Implementation Results

The following are sample ASIC pre-layout results and do not represent the absolute highest speed or smallest area possible. (Area figures do not include memories.)

	Technology	Clock Frequency	Area
T80251XC3–CPU (CPU-only)	40nm	532 MHz	15,630 eq. Gates

Deliverables

The core is available in Verilog RTL or as a targeted FPGA netlist. Its deliverables include everything required for a successful implementation, including a behavioral model, an automated constrained random verification (CRV) testbench, comprehensive documentation, and sample synthesis and simulation scripts.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available; contact CAST Sales.