SPMI-CTRL

MIPI SPMI Master or Slave Controller

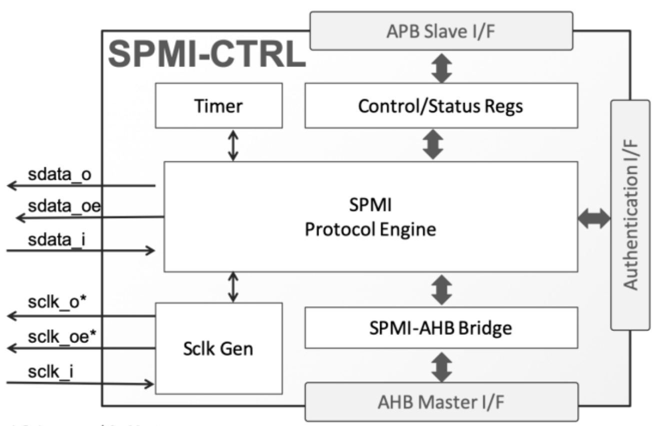
The SPMI-CTRL core implements a highly featured, easy-to-use controller for the MIPI System Power Management Interface (MIPI-SPMI) bus. It supports the latest version (v2.0) of the MIPI-SPMI specification, and is suitable for the implementation of either master or slave nodes in an SPMI bus.

The core is designed to minimize the software load on the host processor. Once configured, the core requires no assistance from the host to initialize the bus, connect to bus or disconnect from the bus, grant access of the bus, execute incoming SPMI commands, generate ACK/NACK responses, and check address and data parity.

Although the core only expects the host to provide the outgoing SPMI commands, it provides thorough status information to the host, which can be used for a higher application layer or for debugging purposes. Last received command, outgoing command status, bus status, and node operation status are made available to the host via the core's registers. Parity errors, unknown commands, or failure of receiving node to provide ACK/NACK response are also reported. Furthermore, the core can be programmed to operate in debug mode, under which the core captures and reports all SPMI bus commands regardless of the destination address.

Integration of the core is extremely simple: The core provides access to its registers via a AMBA™ 2 APB slave interface, and converts the incoming SPMI read/write commands to accesses on its AHB master port. This SPMI-AHB bridging allows easy mapping of the SPMI address space to shared memories or peripheral registers. A dedicated interface allows integration with application specific authentication logic, which can be reduced to just hardwiring the authentication response data. The core uses separate clocks for its APB and AHB bus interfaces, and a separate reference clock source for its internal timer. Clocks are independent to each other, with clean clock domain crossing boundaries, and the only requirement is that the AMBA interface clocks have a frequency larger or equal to the maximum SPMI clock frequency. .

Block Diagram



* Only present for Master core

Verification

The core has been rigorously verified through extensive synthesis, place and route, simulation. It has been proven in both ASIC and FPGA technologies.

FEATURES

MIPI-SPMI v2.0 Master or Slave

- Supports High Speed (HS) and Low Speed (LS) device classes
- Serial clock frequencies from 32kHz to 26MHz
- Supports all commands, including Block, Extended and Extended Long Read/Writes
- Supports all arbitration levels. Suitable for multi-master and/or multi-slave buses.
- Configurations:
  - Arbitration-Capable Master
  - Non-Arbitration-Capable Master
  - Request-Capable Slave
  - Non-Request-Capable Slave

Low Host Overhead

- Autonomously performs bus initialization, bus connect/disconnect, and bus arbitration
- Autonomously executes all incoming SPMI commands, and generates ACK/NACK responses
- Host is only required to: a) initialize register values after a reset b) define outgoing commands and arbitration levels and c) optionally respond to reported errors.

Run-time Debugging Features

- Broadcasts SPMI bus state and device state
- Detects and reports parity, bus or command errors
- Under debug mode captures all traffic in the SPMI bus
- Run-time programmable identifiers (Master, Slave and up to 6 Group Slave Identifiers per device)

Easy Integration

- Directly bridges SPMI and AHB bus address space, allowing SPMI address space mapping to either a shared memory or directly to peripheral registers
- Register access via 32-bit AMBA™ 2 APB bus

Small and Low Power

- Less than 900 LUTs for either the master or the slave core
- Direct serial clock usage to minimize switching activity when idle

Deliverables

- Verilog RTL or targeted netlist
- Testbench
- Sample synthesis and simulation scripts
- Comprehensive documentation

Size and Performance

The SPMI-CTRL can be mapped to any Lattice FPGA device, provided sufficient resources are available. The following table provides sample resource utilization data. Please contact CAST to get characterization data for your target device and technology.

Configuration	Family	Logic Resources
Non-Arbitration-Capable Master	ECP5	1,269 LUT4s / 646 Slices
Request-Capable Slave		2,556 LUT4s / 1,296 Slices
Non-Request-Capable Slave		1,188 LUT4s / 610 Slices
Arbitration-Capable Master	MachXO2	2,724 LUT4s / 1,375 Slices
Non-Arbitration-Capable Master		1,274 LUT4s / 644 Slices
Arbitration-Capable Master	iCE40 HX	3,237 LUTs / 3,247 LCs
Non-Arbitration-Capable Master		1,474 LUTs / 1,477 LCs
Request-Capable Slave		2,893 LUTs / 2,808 LCs
Non-Request-Capable Slave		1,346 LUTs / 1,346 LCs

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

Deliverables

The core is available in synthesizable RTL and FPGA netlist forms, and includes everything required for successful implementation, including:

- Verilog RTL source code or Targeted FPGA Netlist
- System Verilog Testbench
- Simulation scripts
- Synthesis scripts
- Documentation