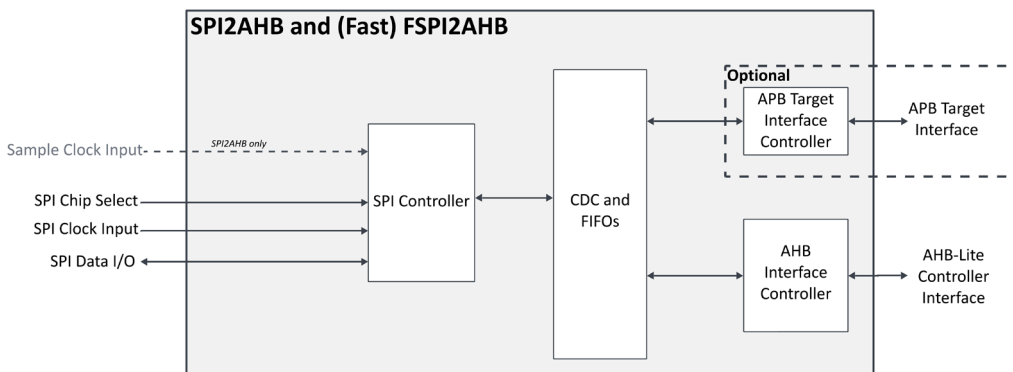# SPI2AHB
SPI to AHB-Lite Bridge

The SPI2AHB core implements an SPI slave to AHB-Lite master bridge. It allows an external SPI master to perform read or write access to any memory-mapped device on the internal AHB bus.

The core implements a simple over-SPI protocol to convert SPI transactions into AHB Read or Write instructions. This over-SPI protocol supports variable-length data accesses, which are translated to AHB-Lite accesses on the AHB-Lite master port. The bridge also monitors the AHB-Lite bus and reports erroneous transfers to the system. Errors captured by the core include Error Responses on the AHB bus, and errors due to slow responses for the accessed AHB-Lite slave.

The core supports single, dual, quad, and octal SPI data lines. The lower-level SPI transmission format is compliant to the SPI de facto standard but fixed to minimize area and power. The core drives the outbound serial data on the rising edge of the serial clock, and samples inbound serial data on the negative edge of the serial clock (CPHA=1) while the resting state of the serial clock is low (CPOL=0).

The SPI2AHB is designed using industry best practices. Its reliability and low risk have been proven through both rigorous verification and customer production. It is available in Verilog RTL source or as a targeted FPGA netlist, and its deliverables include sample synthesis and simulation scripts and comprehensive user documentation.

Block Diagram

Versions

The SPI2AHB core is available in two versions: the standard (SPI2AHB) and the fast (FSPI2AHB). The differences between the two versions are:

1. The fast version supports both a 32-bit and 64-bit AHB-lite bus, while the standard version supports only 32-bit
2. The fast version is partially clocked by the serial SPI clock and an inverted version of it. The standard version treats the serial clock as a data line that is sampled using an externally provided clock, which needs to be at least 8 times faster than the serial SPI clock. Constraining the fast version is therefore a bit more demanding than constraining the standard version, as CDC boundaries must be properly managed and constrained due to the asynchronous nature of SPI and the internal AHB clocks
3. The fast version supports data-strobe (DQS) signals, while the standard version does not
4. The fast version supports byte-level access while the standard supports only word-level access

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Applications

The SPI2AHB enables an external device to have full access to the internal AHB-Lite bus over an SPI connection. It can be used for firmware uploads, design initialization, and run-time monitor, control, and debug in a wide variety of designs including typical micro-controllers, sensors, MEMs, and analogue front ends.

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

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