SPI2AHB

SPI to AHB-Lite Bridge

The SPI2AHB core implements an SPI slave to AHB-Lite master bridge. It allows an external SPI master to perform read or write access to any memory-mapped device on the internal AHB bus.

The core implements a simple over-SPI protocol to convert SPI transactions into AHB Read or Write instructions. This over-SPI protocol supports only 32-bit wide data accesses, which are translated to AHB-Lite accesses on the AHB-Lite master port. The bridge also monitors the AHB-Lite bus and reports erroneous transfers to the system. Errors captured by the core include Error Responses on the AHB bus, and errors due to slow responses for the accessed AHB-Lite slave.

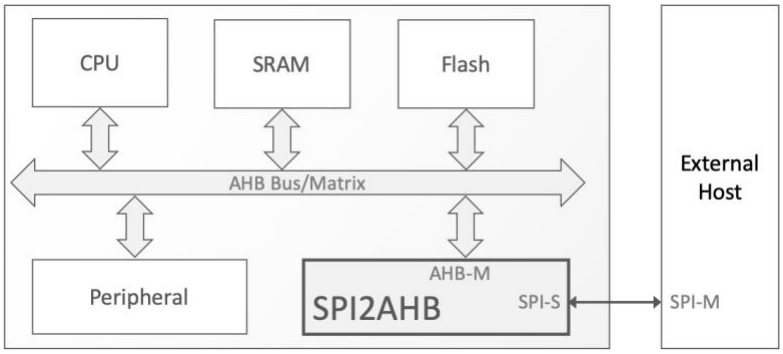
The core supports single, dual, quad, and octal SPI data lines. The lower level SPI transmission format is compliant to the SPI de facto standard, but fixed to minimize area and power. The core drives the outbound serial data on the rising edge of the serial clock, and samples inbound serial data on the negative edge of the serial clock (CPHA=1) while the resting state of the serial clock is low (CPOL=0). Furthermore, all SPI transactions are assumed to be 32 bits wide.

The SPI2AHB is designed with industry best practices, and its reliability and low risk have been proven through both rigorous verification and customer production. It is available in Verilog RTL source or as a targeted FPGA netlist, and its deliverables include sample synthesis and simulation scripts and comprehensive user documentation.

Applications

The SPI2AHB enables an external device to have full access to the internal AHB-Lite bus over an SPI connection. It can be used for firmware uploads, design initialization, and run-time monitor, control, and debug in a wide variety of designs including typical microcontrollers, sensors, MEMs, and analogue front ends.

Block Diagram



FEATURES

Enables an external device to have full access to the internal AHB-Lite bus over an SPI connection.

Typical Use-Cases

- Firmware upload over SPI
- Monitor and Control over SPI
  - e.g. Analog Front End or MEMs initialization and calibration over SPI
- Debug Over SPI

Interfaces

- SPI-Slave Interface
  - Single, Dual, Quad, and Octal serial data lines
  - 32-bit SPI transfers
  - Fixed transmission format (CPOL=0, CPHA=1) for lower area and power
- AHB-Lite Master Interface
- Optional APB slave interface for register access

Easy Integration

- Independent serial and system (AHB bus) clocks
- CDC-Clean design: Signals crossing clock domains are doubled buffered in the destination domain
- Bus Error Reporting
  - Core monitors the AHB Lite bus and reports erroneous transfers and error type to registers accessible via SPI and via an APB interface.

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- User Documentation
- Sample synthesis and simulation scripts

Support

The core as delivered is warranted against defects for ninety days from purchase. Thirty days of phone and email technical support are included, starting with the first interaction. Additional maintenance and support options are available.

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